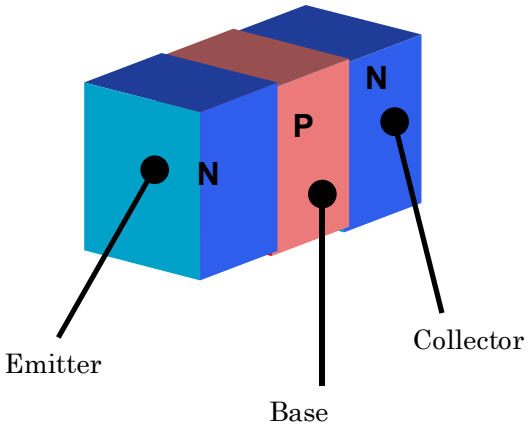
EET-225 Homework #3
Sr. Professor Wheeler

1. Draw a diagram illustrating the construction of a bipolar junction transistor (BJT). Clearly label the electrode names. What are the two types (polarities) of BJTs?



The figure above is a "textbook" representation of an NPN BJT. The two types of BJTs are NPN and PNP. (NPN is shown).

2. Describe the function of each of the three electrodes of a BJT.

a) The *base* is the control electrode. Its current controls whether the transistor is on or off.

b) The *emitter* and *collector* electrodes pass the current being controlled. The emitter current is the sum of all transistor currents.

3. Explain each of the following BJT ratings. If a formula is associated with the rating, state it.

a) β_{DC} (h_{FE}) is the current gain of the transistor. $\beta_{DC} = \frac{I_C}{I_B}$

b) α_{DC} is the ratio of collector to emitter current. $\alpha_{DC} = \frac{I_C}{I_E} = \frac{\beta_{DC}}{\beta_{DC}+1}$

c) V_{CEO} is the maximum voltage allowed between the collector and emitter terminals with the base terminal open circuited.

d) $I_{C(MAX)}$ is the maximum continuous DC collector current.

e) P_D is the maximum allowed power dissipation. $P_D = V_{CE} I_C$

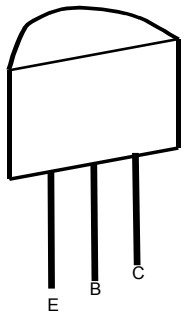
f) β is the current gain for AC signals. AC Beta is frequency dependent - it falls with increasing frequency.

g) $V_{CE(SAT)}$ is the collector-emitter voltage expected when the transistor is fully turned on. It is usually 0.1 - 0.2 volts.

h) F_T is the unity-gain frequency for the transistor. At this frequency, the current gain (Beta) becomes unity. Above this frequency, the transistor produces signal *loss* instead of signal gain.

4. Look up the following ratings and information for a 2N3904 NPN transistor using a databook or manufacturer's web site. Fairchild semiconductor is one manufacturer of this device (http://www.fairchildsemi.com).

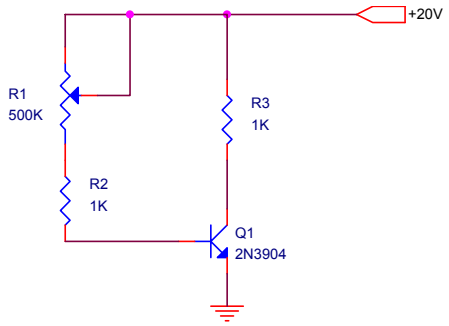
a) Pin-out -- Sketch the device and show how to locate the three electrodes



b) The possible range of values for β_{DC} (h_{FE}) for I_C = 10 mA is from 100 to 300.
c) $V_{CE(SAT)}$ is given as 0.2 to 0.3 V for I_C in the range of 10-50 mA.
d) $I_{C(MAX)}$ is given as 200 mA
e) P_D is given as 625 mW (derate 5 mW/degree C above 25 degrees C)

5. The circuit below uses a variable resistor to vary the base "drive" level to a NPN transistor with a β_{DC} (h_{FE}) of 150. Calculate the collector current that will flow for the following three conditions and plot the load line for the collector-emitter circuit.

a) R1 at minimum value b) R1 at maximum value c) R1 at mid value



For all three conditions, the collector saturation current is:

$$I_{C(SAT)} = \frac{V_{CC}}{R_C + R_E} = \frac{20V}{1K + 0} = 20mA$$

This means that no more than 20 mA can flow in the collector-emitter circuit at any time, and it also defines one end of the load line.

Also, the collector-emitter cutoff voltage is:

$$V_{CE(OFF)} = V_{CC} = 20V$$

This defines the other end of the load line.

a) With R1 at minimum value:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20V - 0.7V}{1K} = 19.3mA$$

$$I_C = \beta I_B = (150)(19.3mA) = 2.895A$$

This condition is impossible since $I_{C(SAT)}$ is only 20 mA (!), so we know the following:

$I_C = I_{C(SAT)} = \underline{20\ mA}$

a) With R1 at maximum value:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20V - 0.7V}{501K} = 38.5\mu A$$

$$I_C = \beta I_B = (150)(38.5\mu A) = \underline{\underline{5.78mA}}$$

This point is about 1/4 the way up the load line. The transistor is operating in its linear region.

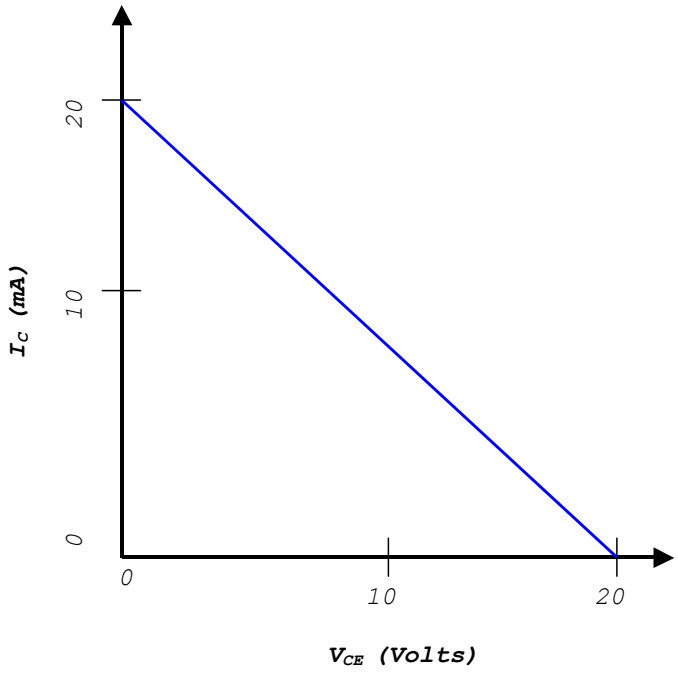
c) With R1 at mid value:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20V - 0.7V}{251K} = 76.89\mu A$$

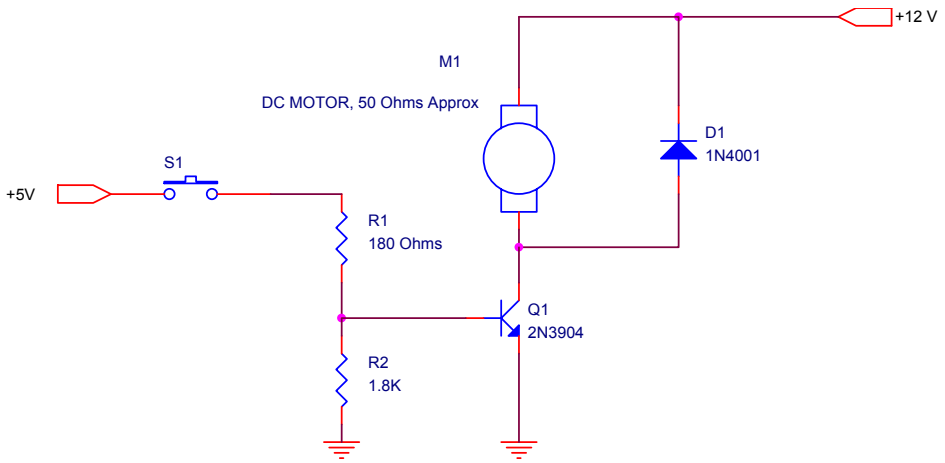
$$I_C = \beta I_B = (150)(76.89\mu A) = \underline{\underline{11.53mA}}$$

This point is a little more than halfway up the load line.

The load line looks like this:



6. The circuit below uses a 2N3904 to switch on a small DC motor (R_{EQUIV} = 50 Ω) when momentary-contact switch S_1 is depressed. Assume that h_{FE} = 100. Diode D1 protects the transistor from the inductive transient that results when the motor is switched off, and can be ignored for this analysis.



Note that the transistor allows a 12 volt motor to be switched by a lower voltage (5V) circuit.

For all cases, the load line ends are found as follows:

$$I_{C(SAT)} = \frac{V_{CC}}{R_C + R_E} = \frac{12V}{50\Omega + 0} = 240mA$$

and

$$V_{CE(OFF)} = V_{CC} = 12V$$

a) Calculate all voltages and currents in the circuit when S_1 is open (not pressed).

By inspection, the following can be noted:

R2 pulls the base voltage down to 0V. This reverse-biases the base-emitter junction, turning the transistor off. Therefore, $\underline{I_B = 0\ mA}$ and $\underline{I_C = 0\ mA}$. The collector voltage pulls up to V_{CC} through the load since no load current is being drawn:

$$V_C = V_{CC} - I_C R_C = 12V - (0mA)(50\Omega) = \underline{12V}$$

b) Calculate all voltages and currents when S_1 is depressed.

When S_1 is pressed, 5V is introduced into the base bias circuit. By Thevenizing the R1-R2 circuit, we get:

$$R_{TH} = R_1 \,||\, R_2 = 1.8K \,||\, 180\Omega = 163.64\Omega$$

$$V_{TH} = V_{IN}\left(\frac{R2}{R1+R2}\right) = 5V\left(\frac{1.8K}{180\Omega+1.8K}\right) = 4.55V$$

The base current can now be determined:

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH}} = \frac{4.55V - 0.7V}{163.64\Omega} = \underline{23.5mA}$$

The collector current is:

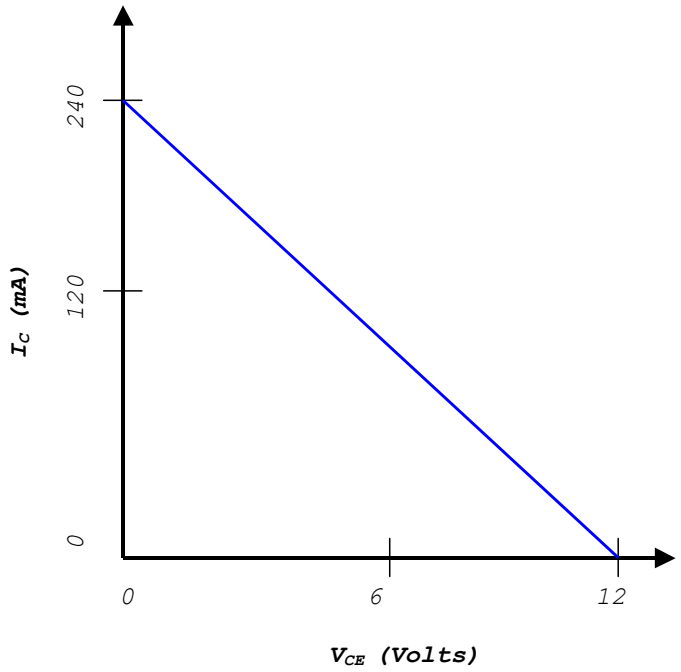
$$I_C = \beta_{DC} I_B = (100)(23.5mA) = 2.35A$$

Since the collector saturation current is only 240 mA, it is impossible for 2.35 A to be flowing. Therefore, $\underline{I_C = 240\ mA}$ (the transistor is in full conduction).

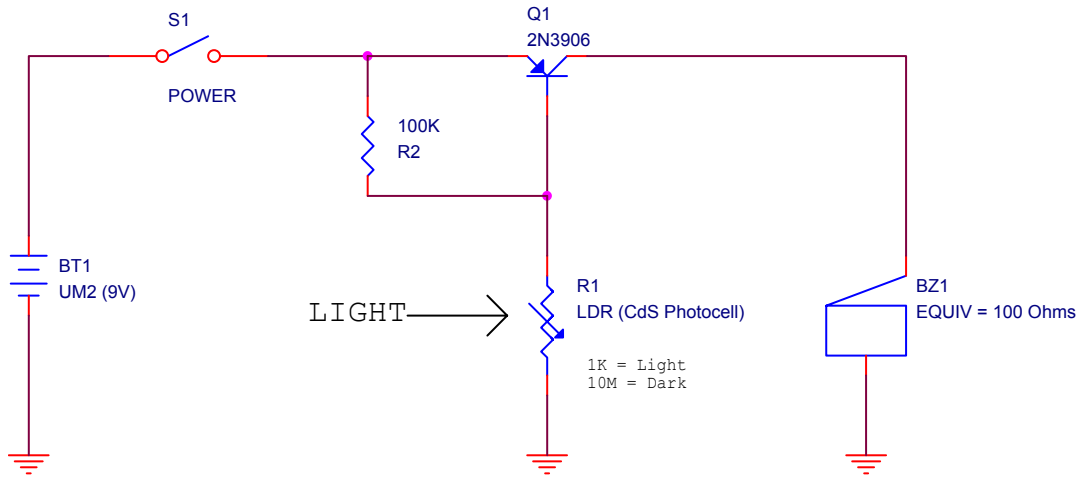
c) What is the purpose of resistors R1 and R2?

R1 determines the base current (drive level) to the transistor in the *on* condition. R2 is a pull-down resistor that forces the transistor off when no voltage is being supplied to the base circuit. Without R2, the transistor might not be fully off due to the effect of I_{CBO} leakage current between collector and base electrodes.

d) Draw the load line for the collector-emitter circuit.



7. The circuit below is a solar-activated "alarm clock." Resistor R1 is a CdS photocell -- a special device with a resistance dependent upon the amount of light striking it. Q1 is a 2N3906 device with a β_{DC} (h_{FE}) of 100.



The operation of the circuit is quite straightforward. Under dark conditions, R1 has a resistance of 10 MΩ, and transistor Q1 is kept off by R2. When sunlight strikes R1, its resistance falls to about 1K Ω, and a base current can then flow in Q1 through R1, which turns Q1 on, in turn supplying power to the buzzer (R_{EQUIV} = 100 Ohms).

a) Calculate all voltages and currents under both "dark" and "light" conditions.

DARK CONDITION: (R1 = 10M)

Resistors R1 and R2 form a voltage divider. The voltage at their junction is the base voltage of Q1. If this voltage more than 8.3 volts, Q1 will be *off* since its base-emitter junction will be reverse-biased. The base voltage of Q1 under this condition is:

$$V_B = V_{TH} = V_{CC}\left(\frac{R_1}{R_1 + R_2}\right) = 9V\left(\frac{10M}{10M + 100K}\right) = \underline{8.91V} \text{ (Q1 VBE < 0.7 V)}$$

<u>The collector voltage of Q1, V_C, is therefore 0V</u> since Q1 is off (non-conducting).

LIGHT CONDITION: (R1 = 1K)

Again the R1-R2 voltage divider is evaluated:

$$V_{TH} = V_{CC}\left(\frac{R_1}{R_1 + R_2}\right) = 9V\left(\frac{1K}{1K + 100K}\right) = \underline{0.089V}$$

This is certainly low enough to turn on Q1, but in order to determine the base current, we must know the Thevenin resistance of the divider:

$$R_{TH} = R_1 \| R_2 = 1K \| 100K = 991\Omega$$

The base current is:

$$I_B = \frac{V_{CC} - V_{BE}}{R_{TH}} = \frac{9V - 0.7V}{991\Omega} = 8.375mA$$

The potential collector current is:

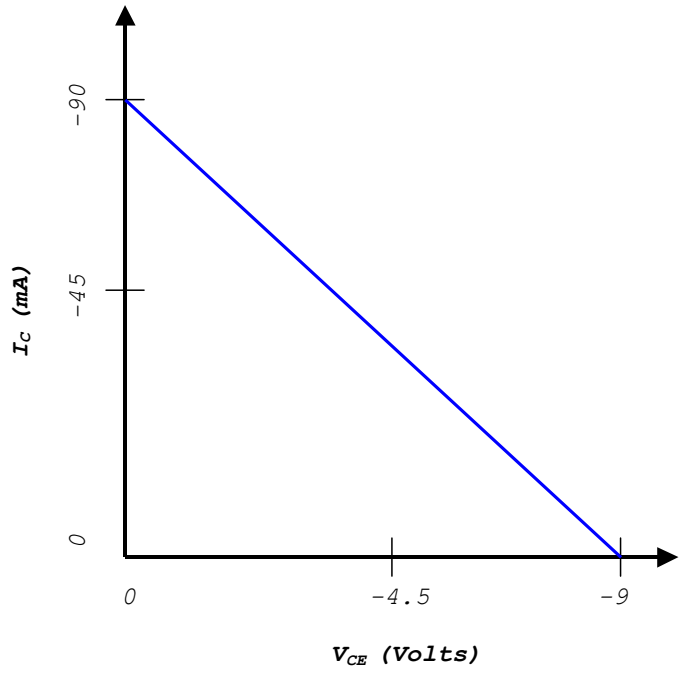
$$I_C = \beta_{DC} I_B = (100)(8.375mA) = 837.5mA$$

This must be checked against the saturation current:

$$I_{C(SAT)} = \frac{V_{CC}}{R_C + R_E} = \frac{9V}{100\Omega + 0} = 90mA$$

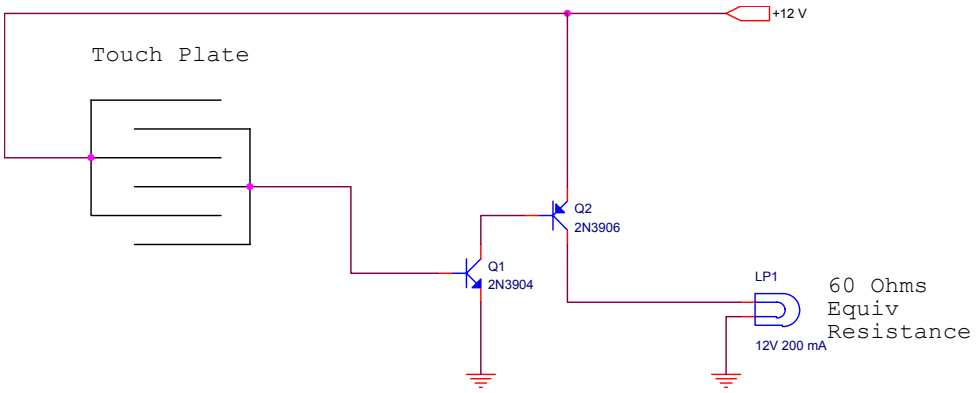
The transistor is therefore in saturation, and $\underline{I_C = 90\ mA}$, and $\underline{V_C = 9V}$. The buzzer will be operating (drawing its 90 mA operating current from the transistor collector).

b) Draw the load line for the collector-emitter circuit.



Note that the voltages and currents here are *negative* since Q1 is a PNP transistor.

8. By cascading transistor stages we can get a circuit of very high sensitivity. The touch-plate in the circuit below presents an open circuit until it is touched by a finger, where it then presents a resistance between 2K and 50KΩ (depending on the user) to the circuit.



The current from the touch-plate is amplified by Q1, then passed to Q2. If Q1 and Q2 both have β_{DC} (h_{FE}) of 100, calculate the load voltage and current if the device is touched by a person with a skin resistance of 40 KΩ.

This circuit must be solved in two stages. First, the base current for Q1 must be found:

$$I_{B1} = \frac{V_{CC} - V_{BE}}{R_{SKIN}} = \frac{12V - 0.7V}{40K} = 282.5\mu A$$

The collector current in Q1 is:

$$I_{C1} = \beta_{DC1} I_{B1} = (100)(282.5\mu A) = 28.25mA$$

This current will become the base current for Q2, since Q1's collector directly drives Q2's base. (The potential saturation current for Q1 will be very large (AMPS!) because of the low DC resistance of Q2's base-emitter diode!)

The potential current in Q2's collector is:

$$I_{C2} = \beta_{DC2} I_{B2} = (100)(28.25mA) = 2.825A$$

This must be compared against the saturation current of Q2:

$$I_{C(SAT)} = \frac{V_{CC}}{R_C + R_E} = \frac{12V}{60\Omega + 0} = 200mA$$

Therefore, Q2 is in full saturation and the full 12 volts @ 200 mA is applied to the lamp.

Note: This circuit has two potential failure modes. First, the saturation current of Q1 is very high because there's no limiting resistor in its collector circuit. If someone with a very low resistance presses on the plate, Q1 may supply enough collector current to damage Q2's base. Also, if someone shorts the touch plate (say with a coin), the full Vcc will be applied across Q1's base-emitter junction, definitely not a healthy outcome!

9. Design a circuit utilizing a 2N3904 to switch a 12V lamp ON when the input voltage supplied to the circuit is a TTL "1" (V_{OH} of TTL logic is 2.4 V). The lamp draws 20 mA. Assume that β_{DC} minimum is 100, and make sure that the transistor is fully saturated.

Design procedure:

1) Determine $I_{C(SAT)}$. In this case, it is equal to the load current (20 mA).

2) Calculate the base current:

$$I_B = \frac{I_C}{\beta} = \frac{20mA}{100} = 200\mu A$$

3) To *guarantee* saturation, *double* the base current:

$$I_{B(SAT)} = 2I_B = 2(200\mu A) = 400\mu A$$

4) Calculate the resistor for driving the base:

$$R_B = \frac{V_{OH}}{I_{B(SAT)}} = \frac{2.4V}{400\mu A} = 6K$$ (Use 5.6K standard value)

(Note that I_{OH} for TTL logic is 400 μA, so the TTL gate can adequately drive the transistor.)

5) Estimate the pull-down resistor:

$$R_{PD} \approx 10R_B \approx 60K$$ (Use 56K standard value)

The schematic of the circuit: