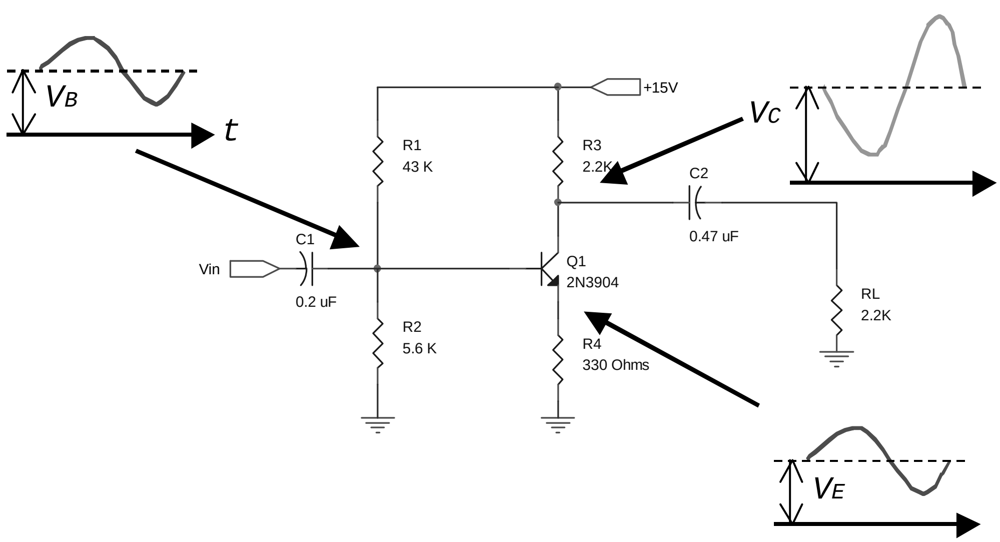
EET-225 Homework #5
Sr. Professor Wheeler

Instructions: This homework must be turned in within a flat 3-tab paper folder (no three-ring binders will be accepted). Answers must be written very neatly or typed. Use complete sentences when answering all questions. Where a problem involves a circuit, you must redraw the circuit as part of the solution, showing all indicated voltages and currents on the circuit diagram. Box or underline all final answers and show all work (see syllabus for example of homework standards).

Use 100 for both Beta DC and Beta AC for all problems in this assignment.

1. Explain how a common-emitter amplifier works by using the "emitter follows base" concept.

The common-emitter amplifier works by allowing the emitter current to be changed (modulated) by an incoming signal at the transistor's base. It works like this:



a) The input signal is clamped to V_B by C1, R1, and R2. C1 allows the AC signal to ride top of the DC voltage V_B. The base voltage is now rising and falling in step with the input signal.

b) The emitter voltage follows the base, lagging by approximately 0.7 V. Therefore the emitter voltage also rises and falls in step with the input signal. This causes the emitter current I_E to vary in step with the input signal as well.

c) Since the collector current is approximately equal to the emitter current, it too varies in step with the input signal. The collector current variations are impressed across the AC equivalent of the collector resistor R_C and the load resistance R_L. In other words, the collector current variations are an AC current that is controlled by the input signal voltage.

d) The AC collector current passing through the collector impedance r_C causes a magnified form of the input signal voltage to appear across the load. Thus, amplification takes place.

2. Give the formula that defines the voltage gain of a circuit. What units are used to denote voltage gain?

The definition of voltage gain is: $A_V = \frac{Vout}{Vin}$

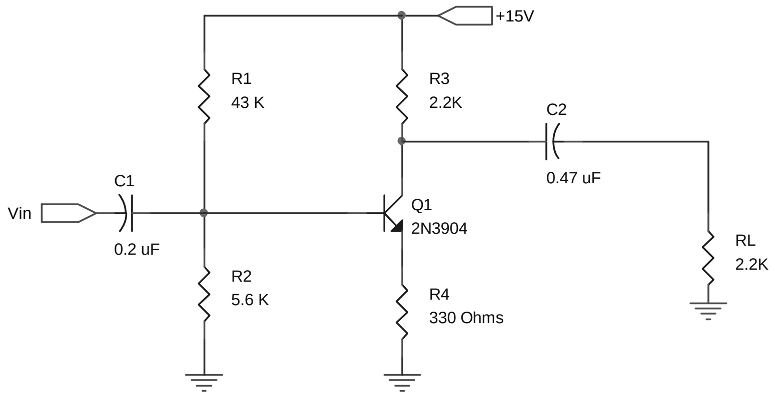
Where *Vin* and *Vout* are the input and output voltages of a circuit.

The *units* of voltage gain are Volts/Volt (V/V).

3. List the three BJT amplifier configurations. For each one, state where the input signal is applied, and where the output is obtained. List at least one characteristic of each configuration. (A table format is strongly suggested).

Amplifier Configuration	**Where input signal is applied**	**Where output is obtained from**	Major Characteristics
Common Emitter	Base	Collector 180° phase shift	Best power gain of all configurations - but worst high-frequency response due to Miller effect
Common Collector	Base	Emitter In phase	Voltage gain approximately 1 V/V in all cases. Provides current gain. Better high frequency response than common-emitter configuration.
Common Base	Emitter	Collector In phase	Best high-frequency response of all configurations, but very low input impedance. Usually seen in RF (radio-frequency) applications as a "front end" amplifier.

4. What is the voltage gain, input impedance, and output impedance of the amplifier below? Show all calculations.



DC Analysis:

$$V_B \approx Vcc\left(\frac{R2}{R1+R2}\right) \approx 15V\left(\frac{5.6K}{5.6K+43K}\right) \approx 1.72V$$

$$V_E = V_B - V_{BE} = 1.72V - 0.7V = 1.02V$$

$$I_E = V_E / R_E = V_E / R4 = 1.02V / 330\Omega = 3.1mA$$

$$V_C = Vcc - I_C R_C = 15V - (3.1mA)(2.2K) = 8.15V$$

AC Analysis:

$$r'e = \frac{25mV}{I_E} = \frac{25mV}{3.1mA} = 8\Omega$$

$$A_V = \frac{r_C}{r_E + r'e} = \frac{R3 \| RL}{R4 + r'e} = \frac{1100\Omega}{330\Omega + 8\Omega} = \underline{\underline{3.25V/V}}$$

$$Z_{IN} = R1 \| R2 \| Z_{IN(BASE)} = R1 \| R2 \| \left(\beta(r_E + r'e)\right) = 43K \| 5.6K \| \left(100(330\Omega + 8\Omega)\right) = \underline{\underline{4321\Omega}}$$

$$Z_{OUT} = R_C = R3 = \underline{\underline{2.2K}}$$

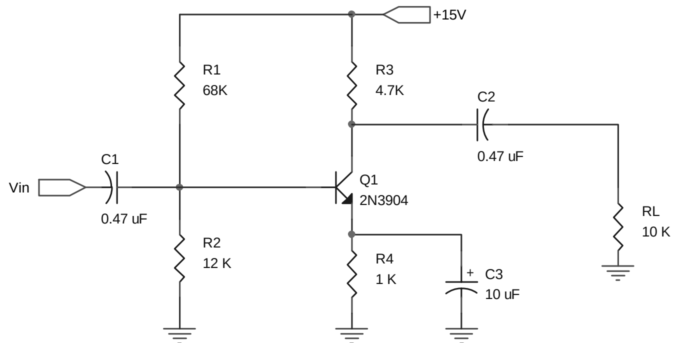
5. Repeat problem 4, but change the load resistor R_L to 4.7K. What happens to the voltage gain, and why?

The DC and AC analysis remain the same, except for the voltage gain which changes as follows:

$$A_V = \frac{r_C}{r_E + r'e} = \frac{R3 \| RL}{R4 + r'e} = \frac{1499\Omega}{330\Omega + 8\Omega} = \underline{\underline{4.43V/V}}$$

The voltage gain *increased* because the load on the amplifier was lightened by increasing the load resistance, which increases the total collector impedance.

6. What is the voltage gain of the amplifier below? Show all calculations.



DC Analysis:

$$V_B \approx Vcc\left(\frac{R2}{R1+R2}\right) \approx 15V\left(\frac{12K}{12K+68K}\right) \approx 2.25V$$

$$V_E = V_B - V_{BE} = 2.25V - 0.7V = 1.55V$$

$$I_E = V_E / R_E = V_E / R4 = 1.55V / 1K\Omega = 1.55mA$$

$$V_C = Vcc - I_C R_C = 15V - (1.55mA)(4.7K) = 7.72V$$

AC Analysis:

$$r'e = \frac{25mV}{I_E} = \frac{25mV}{1.55mA} = 16\Omega$$

$$A_V = \frac{r_C}{r_E + r'e} = \frac{R3 \| RL}{R4 + r'e} = \frac{3197\Omega}{0\Omega + 16\Omega} = \underline{\underline{199.8V/V}}$$

This is an unswamped amplifier. It provides tremendous voltage gain -- but this voltage gain isn't very stable, and the distortion levels are higher than would be encountered with the swamped version.

7. If the emitter current in the amplifier of question 6 were to increase to 2 mA, how would the gain of the unit be affected?

If the emitter current changed to 2 mA, r'e would become 12.5Ω. The voltage gain would become:

$$A_V = \frac{r_C}{r_E + r'e} = \frac{R3 \| RL}{R4 + r'e} = \frac{3197\Omega}{0\Omega + 12.5\Omega} = \underline{\underline{255.76V/V}} \text{ (The gain } \textit{increases!}\text{)}$$

This could happen if the DC beta of the transistor varied, raising the *Q*-point.

8. Define the term *swamping* as applied to a common-emitter amplifier. Why is swamping usually desirable?

Swamping is a gain stabilization method that works by making an external emitter resistance r_E much larger than the internal dynamic emitter resistance r'e of the transistor. Because r_E is large, its effect on gain is much greater than r'e and gain is thus stabilized.

Swamping is desirable for two reasons. First, voltage gain is stabilized and becomes much less dependent on device-to-device parameter variations. Second, the swamping resistor introduces *negative feedback* into the emitter circuit, which reduces distortion of the amplified signal.

9. Calculate the lower cutoff frequency f_{lco} for the output coupling network of the amplifier in problem 4. What is the lowest frequency that is firmly coupled by the network in question?

$$f_{lco} = \frac{1}{2\pi RC} = \frac{1}{2\pi R_{TH} C_{COUPLING}} = \frac{1}{2\pi(R3 + RL)C2}$$

$$f_{lco} = \frac{1}{2\pi(2.2K + 2.2K)(0.47\mu F)} = \underline{\underline{76.9Hz}}$$

At this frequency, the response of the network will be 3 dB down from its maximum value.

The lowest frequency that will be firmly coupled is one decade above the lower cutoff frequency:

$$f_{\min - firm} = 10 f_{lco} = 10(76.9Hz) = \underline{\underline{769Hz}}$$

At 769 Hz, the reactance of the coupling capacitor C2 will be 1/10th the Thevenin resistance it sees (Rth = 4.4K, Xc=440Ω at this frequency), so the circuit will be firmly coupled.

10. In a coupling network having a 10K Thevenin resistance, what minimum capacitance value will provide firm coupling at a frequency of 100 Hz?

To provide firm coupling, Xc <= Rth / 10 <= 10K / 10 <= 1KΩ. The capacitance value that provides this reactance is:

$$C = \frac{1}{2\pi fX} = \frac{1}{2\pi(100Hz)(1K)} = \underline{\underline{1.59\mu F}}$$

11. Construct the DC and AC load lines for the amplifier of problem 4. Calculate the compliance of the amplifier and use this value to determine the maximum power deliverable to the load.

DC Analysis

$$I_{C(SAT)} = \frac{V_{CC}}{R_C + R_E} = \frac{15V}{2.2K + 330\Omega} = \underline{5.92mA}$$

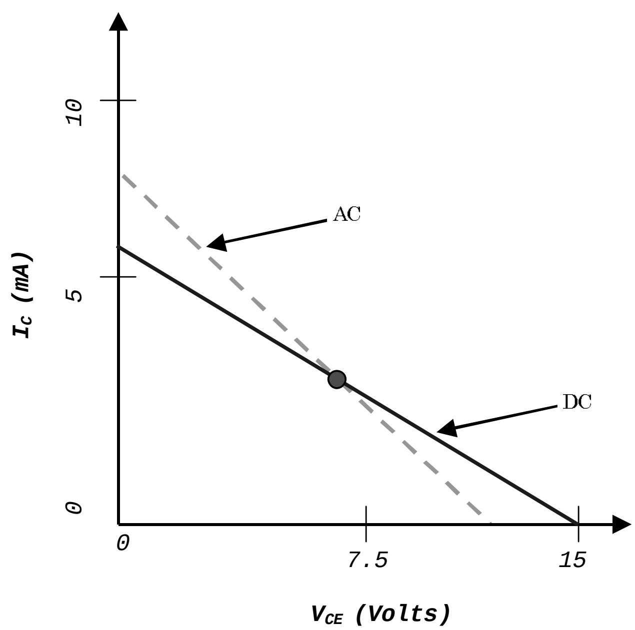
$V_{CE(OFF)} = V_{CC} = \underline{15V}$

AC Analysis (Steady-state DC values were obtained in problem 4)

$$i_{c(sat)} = I_{C(Q)} + \frac{V_{CE(Q)}}{r_E + r_C} = 3.1mA + \frac{(8.15V - 1.02V)}{(330\Omega + 1100\Omega)} = \underline{8.08mA}$$

$$v_{CE(off)} = V_{CE(Q)} + I_{C(Q)}(r_C + r_E) = (8.15V - 1.02V) + (3.1mA)(1100\Omega + 330\Omega) = \underline{11.56V}$$

The load lines look like this:



Compliance and Power Output

$$Vpp = 2Ic(q)r_C = 2(3.1mA)(1100\Omega) = 6.82Vpp$$

$$Vpp = 2Vce(q)\left(\frac{r_C}{r_C + r_E}\right) = 2(8.15V - 1.02V)\left(\frac{1100\Omega}{1100\Omega + 330\Omega}\right) = 10.96Vpp$$

The compliance is the smaller of the two figures, 6.82 Vpp. The available power output is:

$$P_O = \frac{V_{PP}^2}{8R_L} = \frac{(6.82Vpp)^2}{(8)(2.2K)} = \underline{\underline{2.6mW}}$$

12. Design a common-emitter amplifier to meet the following specifications. Show all calculations and the completed schematic of the unit.

$10 <= A_V <= 20$ V/V $R_L = 4.7$ K $f_{lco} <= 100$ Hz
Vpp >= 3 Vpp

Design Procedure:

0) Vcc >= 2 Vpp >= 6V (Will use 8V DC for additional margin)
1) Rc = Zout = R_L = 4.7K
2) V_E = 1 V
3) $r_C = Rc \| RL = 4.7K \| 4.7K = 2350\Omega$
4) $V_{CE(Q)} = \frac{Vcc}{3} = \frac{8V}{3} = 2.66V$ (Gamma = 1/3 to optimize Vpp output swing)
5) $I_E \approx I_C \approx \frac{Vcc - Vc}{Rc} = \frac{Vcc - (V_{CE(Q)} + V_E)}{Rc} = \frac{8V - (2.66V + 1V)}{4.7K} = \underline{0.92mA}$
6) $R_{e1} + R_{e2} = R_E = \frac{V_E}{I_E} = \frac{1V}{0.92mA} = 1082\Omega$
7) $r'e = \frac{25mV}{I_E} = \frac{25mV}{0.92mA} = 27\Omega$
8) $\text{Re1} = \frac{r_c}{Av} - r'e = \frac{2.35K}{15} - 27\Omega = 129.666\Omega$ (120 Ω Std.)
9) $\text{Re2} = R_E - \text{Re1} = 1082\Omega - 120\Omega = 962\Omega$ (1 K Std.)
10) $V_B = V_E + 0.7V = 1.7V$
11) $I_B = I_C / \beta = 0.92mA/100 = 9.2\mu A$
12) $R_{B2} = \frac{V_B}{10I_B} = \frac{1.7V}{92\mu A} = 18.47K\Omega$ (18K Std.)
13) $R_{B1} = \frac{V_{CC} - V_B}{11I_B} = \frac{8V - 1.7V}{101.2\mu A} = 62.252K\Omega$ (56K Std.)

Coupling & Bypass Capacitors

Set Xc to 1/10 of Rth at the lowest frequency (f_{lco}) and calculate capacitors at this frequency. This will result in firm coupling at the lowest frequency (f_{lco}).

Output capacitor: Rth = R_L+R_C = 4.7K + 4.7K = 9.4K; Rth/10 = 940 Ω so Xc<=940Ω @ 100Hz.

$$C2 = \frac{1}{2\pi f_{lco} X_C} = \frac{1}{2\pi(100Hz)(940\Omega)} = \underline{\underline{1.6\mu F}}$$ (2.2 µF Std.)

Input capacitor: Let Rth=Zin of amplifier.

$$Z_{IN} = R1 \| R2 \| Z_{IN(BASE)} = R1 \| R2 \| \left(\beta(r_E + r'e)\right) = 56K \| 18K \| \left(100(120\Omega + 27\Omega)\right) = \underline{\underline{7.07K\Omega}}$$

So Xc<=Rth/10<=707Ω @ 100 Hz:

$$C1 = \frac{1}{2\pi f_{lco} X_C} = \frac{1}{2\pi(100Hz)(707\Omega)} = \underline{\underline{2.25\mu F}} \quad (\underline{2.2\ \mu F\ Std.})$$

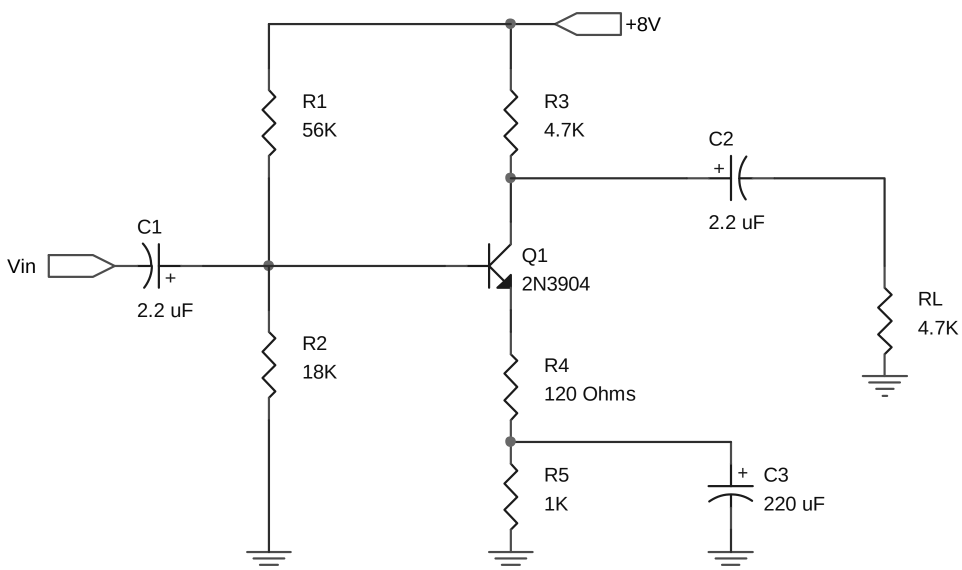
Emitter Bypass Capacitor:

Let Rth = Re2 | | (Re1 + r'e) = 1K | | (120 Ω+ 27 Ω) = 128 Ω

So Xc<=Rth/10<=12.8Ω @ 100 Hz:

$$C3 = \frac{1}{2\pi f_{lco} X_C} = \frac{1}{2\pi(100Hz)(12.8\Omega)} = \underline{\underline{124\mu F}} \quad (\underline{220\ \mu F\ Std.})$$

The schematic of the unit looks like this:



13. Design a common-emitter amplifier to meet the following specifications. Show all calculations and the completed schematic of the unit.

$20 <= A_V <= 25$ V/V
$R_L = 2.2$ K
$f_{lco} <= 10$ Hz
Vpp >= 10 Vpp

Design Procedure:

0) Vcc >= 2 Vpp >= 20V (Will use 20V DC)
1) Rc = Zout = R_L =2.2K
2) V_E = 1 V
3) $r_C = Rc \| RL = 2.2K \| 2.2K = 1100\Omega$
4) $V_{CE(Q)} = \frac{Vcc}{3} = \frac{20V}{3} = 6.6\overline{6}V$ (Gamma = 1/3 to optimize Vpp output swing)
5) $I_E \approx I_C \approx \frac{Vcc - Vc}{Rc} = \frac{Vcc - (V_{CE(Q)} + V_E)}{Rc} = \frac{20V - (6.66V + 1V)}{2.2K} = \underline{5.6mA}$
6) $R_{e1} + R_{e2} = R_E = \frac{V_E}{I_E} = \frac{1V}{5.6mA} = 178\Omega$
7) $r'e = \frac{25mV}{I_E} = \frac{25mV}{5.6mA} = 4.5\Omega$
8) $\text{Re1} = \frac{r_c}{Av} - r'e = \frac{1.1K}{23} - 4.5\Omega = 43.326\Omega$ (47 **Ω** Std.)
9) $\text{Re2} = R_E - \text{Re1} = 178\Omega - 47\Omega = 131\Omega$ (120**Ω** Std.)
10) $V_B = V_E + 0.7V = 1.7V$
11) $I_B = I_C / \beta = 5.6mA/100 = 56\mu A$
12) $R_{B2} = \frac{V_B}{10 I_B} = \frac{1.7V}{560\mu A} = 3.036K\Omega$ (2.7K Std.)
13) $R_{B1} = \frac{V_{CC} - V_B}{11 I_B} = \frac{20V - 1.7V}{616\mu A} = 29.707K\Omega$ (27K Std.)

Coupling & Bypass Capacitors

Set Xc to 1/10 of Rth at the lowest frequency (f_{lco}) and calculate capacitors at this frequency. This will result in firm coupling at the lowest frequency (f_{lco}).

Output capacitor: Rth = $R_L + R_C$ = 2.2K + 2.2K = 4.4K; Rth/10 = 440 Ω so Xc<=440Ω @ 10Hz.

$$C2 = \frac{1}{2\pi f_{lco} X_C} = \frac{1}{2\pi(10Hz)(440\Omega)} = \underline{\underline{36\mu F}}$$ (47 µF Std.)

Input capacitor: Let Rth=Zin of amplifier.

$$Z_{IN} = R1 \| R2 \| Z_{IN(BASE)} = R1 \| R2 \| \left(\beta(r_E + r'e)\right) = 27K \| 2.7K \| \left(100(47\Omega + 4.5\Omega)\right) = \underline{\underline{1.662K\Omega}}$$

So Xc<=Rth/10<=166Ω @ 10 Hz:

$$C1 = \frac{1}{2\pi f_{lco} X_C} = \frac{1}{2\pi(10Hz)(166\Omega)} = \underline{\underline{95.8\mu F}} \quad (\underline{100\ \mu\text{F Std.}})$$

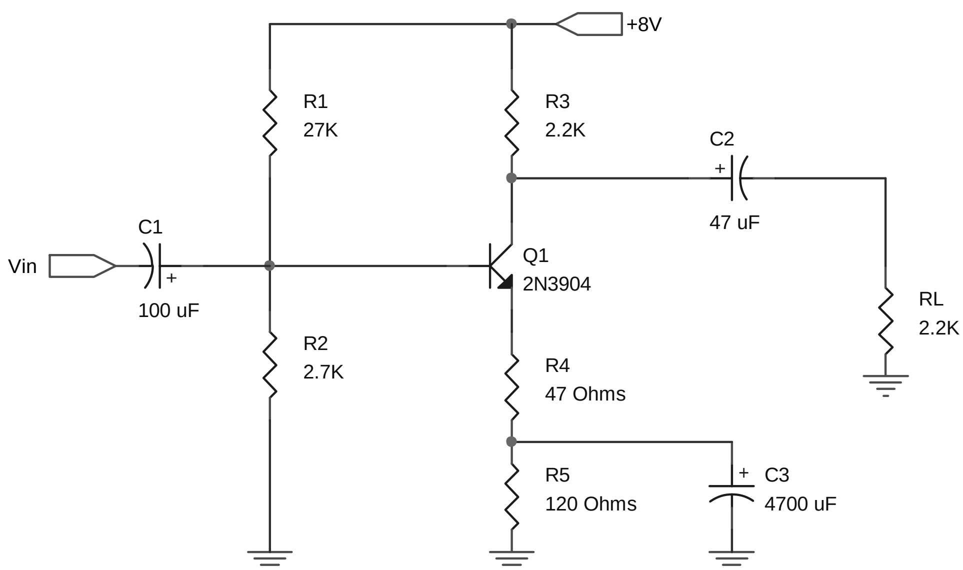
Emitter Bypass Capacitor:

Let Rth = Re2 | | (Re1 + r'e) = 120Ω | | (47 Ω+ 4.5 Ω) = 36 Ω

So Xc<=Rth/10<=3.6Ω @ 10 Hz:

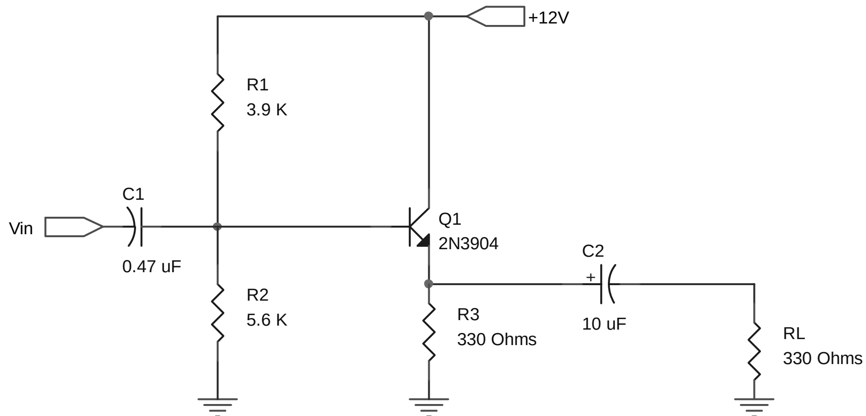
$$C3 = \frac{1}{2\pi f_{lco} X_C} = \frac{1}{2\pi(10Hz)(3.6\Omega)} = \underline{\underline{4420\mu F}} \quad (\underline{4700\ \mu\text{F Std.}})$$

The schematic of the unit looks like this:



Note how the capacitors are getting HUGE in size. This is a problem for low-frequency amplifiers. These capacitors are expensive and take up a considerable amount of space. It is solved quite nicely by *direct-coupling* techniques which DC-couple amplifier stages into each other, eliminating the capacitors altogether.

14. Analyze the common-collector amplifier below and determine the following: Voltage gain, input impedance, output impedance, compliance. Draw the DC and AC load lines for the unit.



DC Analysis:

$$V_B \approx Vcc\left(\frac{R2}{R1+R2}\right) \approx 12V\left(\frac{5.6K}{5.6K+3.9K}\right) \approx 7.07V$$

$$V_E = V_B - V_{BE} = 7.07V - 0.7V = 6.37V$$

$$I_E = V_E / R_E = V_E / R4 = 6.37V / 330\Omega = 19.3mA$$

$$V_C = Vcc = 12V$$

AC Analysis:

$$r'e = \frac{25mV}{I_E} = \frac{25mV}{19.3mA} = 1.3\Omega$$

$$A_V = \frac{r_E}{r_E + r'e} = \frac{R3 \,||\, RL}{R3 \,||\, RL + r'e} = \frac{165\Omega}{165\Omega + 1.3\Omega} = \underline{\underline{0.99V/V}}$$

$$Z_{IN} = R1 \,||\, R2 \,||\, Z_{IN(BASE)} = R1 \,||\, R2 \,||\, (\beta(r_E + r'e)) = 3.9K \,||\, 5.6K \,||\, (100(165\Omega + 1.3\Omega)) = \underline{\underline{2019\Omega}}$$

$$Z_{OUT} = r'e \,||\, R_E = 1.3\Omega \,||\, 330\Omega \approx \underline{\underline{1.3\Omega}}$$

$$Vpp = 2Ic(q)r_E = 2(19.3mA)(165\Omega) = 6.37Vpp$$
$$Vpp = 2Vce(q) = 2(12V - 6.37V) = 11.26Vpp$$

The compliance is the smaller of the two or $\underline{\underline{\text{6.37 Vpp}}}$.

$$I_{C(SAT)} = \frac{V_{CC}}{R_C + R_E} = \frac{12V}{0\Omega + 330\Omega} = \underline{36.3mA}$$

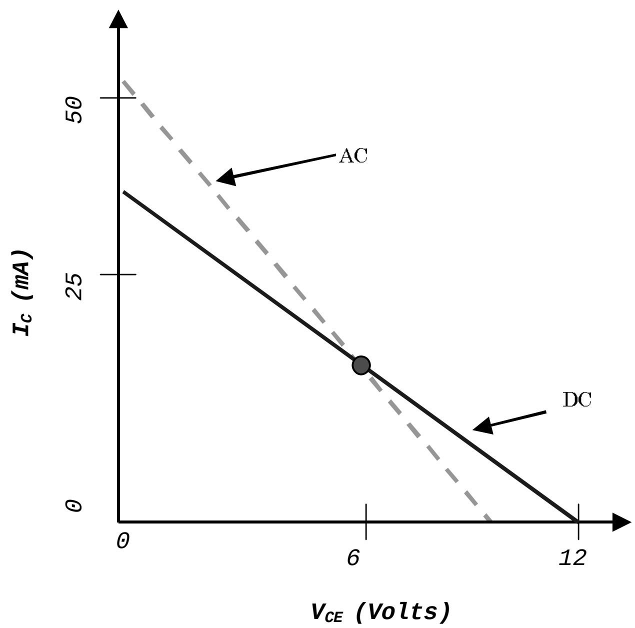
$V_{CE(OFF)} = V_{CC} = \underline{12V}$

AC Analysis

$$i_{c(sat)} = I_{C(Q)} + \frac{V_{CE(Q)}}{r_E + r_C} = 19.3mA + \frac{(12V - 6.37V)}{(165\Omega + 0\Omega)} = \underline{53.4mA}$$

$$v_{CE(off)} = V_{CE(Q)} + I_{C(Q)}(r_C + r_E) = (12V - 6.37V) + (19.3mA)(0\Omega + 165\Omega) = \underline{8.82V}$$

The load lines look like this:



15. Design a common-collector amplifier to meet the following specifications. Show all calculations and the completed schematic of the unit.

$A_V \cong 1$ V/V
$R_L = 75\ \Omega$
Vcc = 5 V
Vpp (compliance) >= 2 Vpp
f_{lco} <= 30 Hz

Design Procedure:

0) Vcc >= 2 Vpp >= 4V (Will use <u>5V</u> DC)
1) $R_E = R_L = 75\ \Omega$
2) V_E = 2/3 Vcc = 3.33 V (Sets Gamma = 1/3 to optimize Vpp output swing)
3) $r_E = R_E \| R_L = 75\Omega \| 75\Omega = 37.5\Omega$
4) $I_E = \dfrac{V_E}{R_E} = \dfrac{3.33V}{37.5\Omega} = 88.8\bar{8}mA$
5) $I_B \approx I_E / \beta = 88.8\bar{8}mA/100 = 888\mu A$
6) $V_B = V_E + 0.7V = 3.33V + 0.7V = 4.03V$
7) $R_{B2} = \dfrac{V_B}{10I_B} = \dfrac{4.03V}{8.88mA} = 453.75\Omega$ (<u>470 Ω Std.</u>)
8) $R_{B1} = \dfrac{V_{CC} - V_B}{11I_B} = \dfrac{5V - 3.33V}{9.76mA} = 170.62\Omega$ (<u>180 Ω Std.</u>)
9) $r'e = \dfrac{25mV}{I_E} = \dfrac{25mV}{88.88mA} = 0.28\Omega$

Coupling & Bypass Capacitors

Set Xc to 1/10 of Rth at the lowest frequency (f_{lco}) and calculate capacitors at this frequency. This will result in firm coupling at the lowest frequency (f_{lco}).

Output capacitor: Rth = r'e | | R_L+R_C = (0.28 Ω | | 75 Ω) + 75 Ω = 75 Ω; Rth/10 = 7.5 Ω so Xc<=7.5Ω @ 30Hz.

$$C2 = \frac{1}{2\pi f_{lco} X_C} = \frac{1}{2\pi(30Hz)(7.5\Omega)} = \underline{\underline{707.35\mu F}}$$ (<u>1000 µF Std.</u>)

Input capacitor: Let Rth=Zin of amplifier.

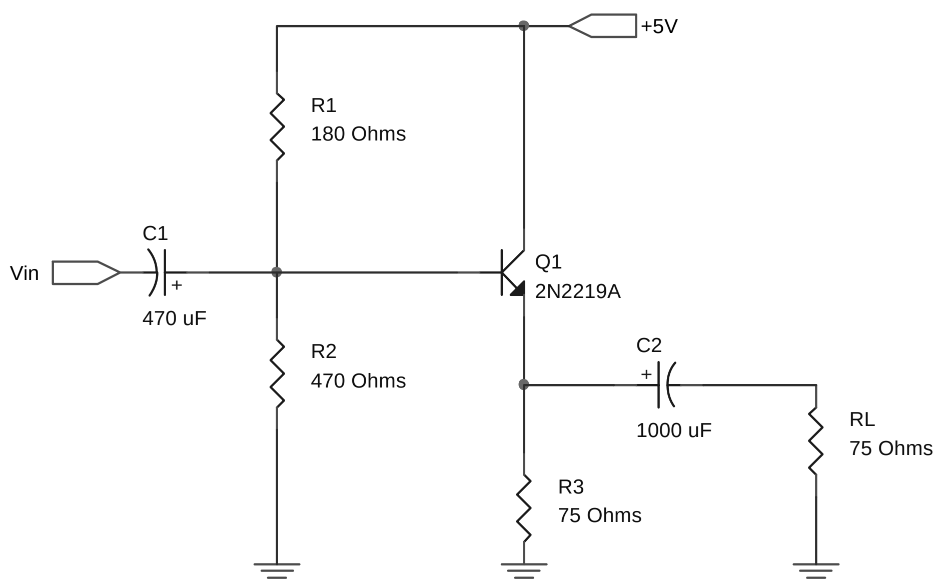
$$Z_{IN} = R1 \| R2 \| Z_{IN(BASE)} = R1 \| R2 \| \left(\beta(r_E + r'e)\right) = 470\Omega \| 180\Omega \| \left(100(37.5\Omega + 0.28\Omega)\right) = \underline{\underline{125.82\Omega}}$$

So Xc<=Rth/10<=12.5Ω @ 30 Hz:

$$C1 = \frac{1}{2\pi f_{lco} X_C} = \frac{1}{2\pi(30Hz)(12.5\Omega)} = \underline{\underline{424\mu F}} \quad (\underline{470\ \mu\text{F Std.}})$$

<u>Note about optimizing input impedance</u>: If you examine the Z_{IN} value for this stage, you'll notice that the base biasing resistors R1 and R2 drastically reduce the Z_{IN} value. ($Z_{IN(BASE)}$ is 3.7 K Ω). This is a good example of a case where using 10 I_B and 11 I_B for the base biasing resistors is a little drastic. Sure, the *Q*-point is rock stable, but the input impedance is also unnecessarily low! Using perhaps 3 I_B and 4 I_B would yield a much higher Z_{IN} while keeping the DC bias relatively stable.

The schematic of the unit looks like this:



16. Design a common-base amplifier to meet the following specifications. Show all calculations and the completed schematic of the unit.

$10 <= A_V <= 15$ V/V
$R_L = 1000\ \Omega$
Vcc = 5 V
$f_{lco} <= 1$ MHz

Design Procedure:

0) Vcc 5 V (Given)
1) Rc = Zout = R_L =1K
2) V_E = 1 V
3) $r_C = Rc \| RL = 1K \| 1K = 500\Omega$
4) $V_{CE(Q)} = \frac{Vcc}{3} = \frac{5V}{3} = 1.6\bar{6}V$ (Gamma = 1/3 to optimize Vpp output swing)
5) $I_E \approx I_C \approx \frac{Vcc - Vc}{Rc} = \frac{Vcc - (V_{CE(Q)} + V_E)}{Rc} = \frac{5V - (1.6\bar{6}V + 1V)}{1K} = \underline{2.33mA}$
6) $R_{e1} + R_{e2} = R_E = \frac{V_E}{I_E} = \frac{1V}{2.33mA} = 428.57\Omega$
7) $r'e = \frac{25mV}{I_E} = \frac{25mV}{2.33mA} = 10.7\Omega$
8) $\text{Re1} = \frac{r_c}{Av} - r'e = \frac{500\Omega}{12.5} - 10.7\Omega = 29.3\Omega$ (27 Ω Std.)
9) $\text{Re2} = R_E - \text{Re1} = 428.57\Omega - 27\Omega = 401.57\Omega$ (390Ω Std.)
10) $V_B = V_E + 0.7V = 1.7V$
11) $I_B = I_C / \beta = 2.33mA/100 = 23.3\mu A$
12) $R_{B2} = \frac{V_B}{10 I_B} = \frac{1.7V}{233\mu A} = 7.286K\Omega$ (6.8K Std.)
13) $R_{B1} = \frac{V_{CC} - V_B}{11 I_B} = \frac{5V - 1.7V}{256.6\mu A} = 12.857K\Omega$ (12K Std.)

Coupling & Bypass Capacitors

Set Xc to 1/10 of Rth at the lowest frequency (f_{lco}) and calculate capacitors at this frequency. This will result in firm coupling at the lowest frequency (f_{lco}).

Output capacitor: Rth = R_L+R_C = 1K + 1K = 2K; Rth/10 = 200 Ω so Xc<=200Ω @ 1 MHz.

$$C2 = \frac{1}{2\pi f_{lco} X_C} = \frac{1}{2\pi(1MHz)(200\Omega)} = \underline{\underline{795pF}}$$ (1 nF (1000 pF) Std.)

Input capacitor: Let Rth=Zin of amplifier.

$$Z_{IN} \approx \mathrm{Re1} \| \mathrm{Re2} \approx 27\Omega \| 390\Omega \approx 25.25\Omega$$

So Xc<=Rth/10<=2.52Ω @ 1 MHz:

$$C1 = \frac{1}{2\pi f_{lco} X_C} = \frac{1}{2\pi(1MHz)(2.52\Omega)} = \underline{\underline{63.2nF}}$$ (68 nF Std.)

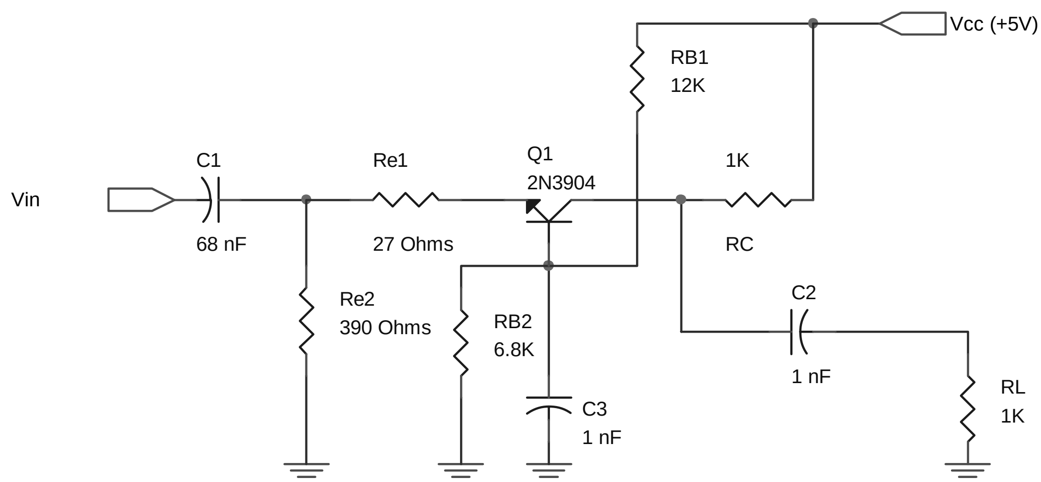
Base Bypass Capacitor:

Let Rth = RB1 | | RB2 | | $Z_{IN(BASE)}$
= 6.8K | | 12 K | | (100)(27 Ω + 10 Ω) = 1997 Ω

So Xc<=Rth/10<=197Ω @ 1 MHz:

$$C3 = \frac{1}{2\pi f_{lco} X_C} = \frac{1}{2\pi(1MHz)(197\Omega)} = \underline{\underline{807\,pF}}$$ (1 nF Std.)

The schematic of the unit looks like this:



Note how the capacitor values are much smaller in this problem. The reason is that the amplifier must pass only *high* frequencies (this is a radio frequency or RF application, so audio frequencies are not to be amplified). At radio frequencies, even a small disc or chip capacitor can provide very effective coupling and feedback because XC is inversely proportional to frequency. It is common for RF engineers to use 0.1 μF and 0.01 μF values as bypass capacitors in their circuits.