EXPERIMENT 6: PHASE LOCKED LOOP

INTRODUCTION:

The phase-locked loop, or PLL, is one of the most useful blocks in modern electronic circuits. It is used in many different applications, ranging from communciations (FM modulation, demodulation, frequency synthesis, signal correlation), control systems (motor control, tracking controls, etc), as well as applications such as pulse recovery and frequency multiplication.

THEORY:

A PLL is a closed-loop system, whose "purpose" is to lock an oscillator onto a provided input frequency (sometimes called the REFERENCE frequency.) By "closed-loop," we mean that there is feedback from output to input. In a PLL, the feedback is negative, meaning that the system is self-correcting. Figure 1 shows the basic elements in a PLL.

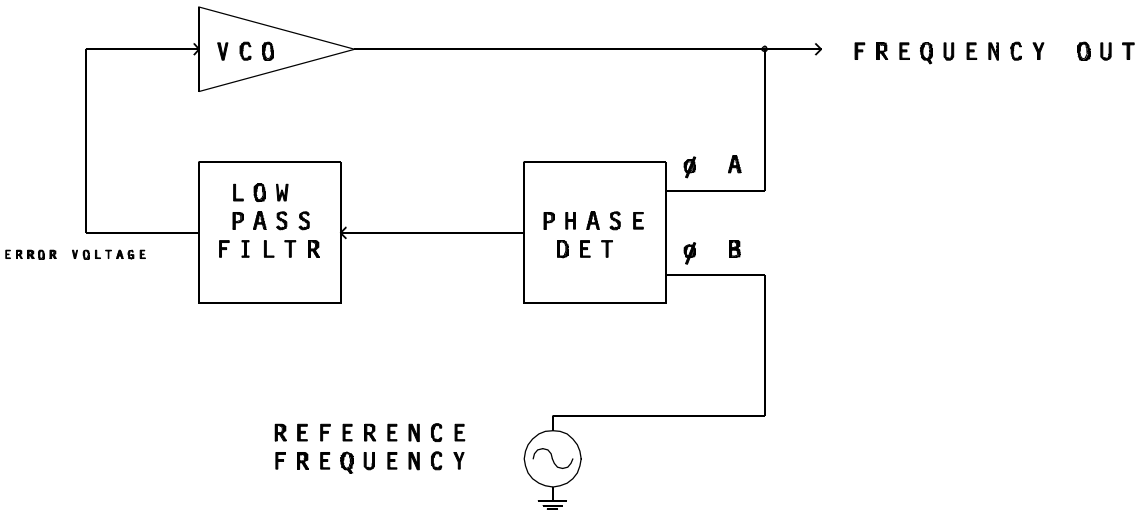

FIGURE 1: PLL BLOCK DIAGRAM

A PLL has a special oscillator called a VCO, or Voltage Controlled Oscillator. The output frequency of the VCO is directly proportional to a *control voltage* that is applied to its input terminal. (It is also dependent upon the values of the timing resistor and capacitor used.) The VCO in effect converts the control *voltage* into *frequency*.

The PLL under normal conditions attempts to make the VCO output frequency exactly equal to a second frequency that is applied to the PLL, the *reference* frequency.

This is acheived by feeding both the VCO output and the reference frequency into a *phase detector*. The phase detector compares the phase of the two waves, and outputs a pulsating-DC waveform with a duty-cycle proportional to the phase difference ("error") between the two signals. Why compare phase and not frequency? Only simple circuitry is required to compare signal phases; and since frequency is the time-derivative of phase, a

constant phase error value produces zero frequency error (the reference and VCO will be *exactly* on the same frequency.)

The output of the phase detector is a pulsating DC with a varying duty cycle. The bigger the phase difference becomes (within certain limits, of course), the larger the duty cycle of the phase detector's output becomes. But the VCO needs a nice, steady DC voltage at its control voltage input. Can you imagine the effect of the pulsating DC on the VCO? Think of a car that only has two throttle positions, wide open and off. It would be nearly impossible to attain a constant speed in such a car because of the crudeness of the control!

The output frequency of the VCO needs to be fairly steady, like the reference input. In order to ensure this, the pulsating DC from the phase detector is fed into a *low-pass filter* on its way to the VCO. This filter in effect "smooths" the rough phase detector output waveform into a fairly steady DC voltage for the VCO. The VCO will then be able to smoothly track the input reference frequency.

PLL STATES

A PLL has three operating states. These are the *free-running, capture,* and *locked* conditions.

In the *free-running* state, there is NO reference input frequency being provided to the PLL. Design constants within the system determine what frequency the VCO will run at. Normally, two of these constants are the values of R_T and C_T, the VCO timing components.

In the *capture* state, which is usually short-lived, the PLL has just been given a reference frequency, and it is in the process of trying to "lock" onto it. The PLL cannot lock onto all frequencies; only a certain range of frequencies, within the *capture range* can be locked onto, if the PLL is initially in the free-running state. Usually, the free-running frequency is in the middle of the capture range. The width of the capture range is determined by PLL design; the loop low-pass filter is important in determining this.

The last PLL state is the desired state: *Locked!* In this state, the PLL has successfully passed through the capture phase, and it has its VCO accurately "locked" onto the input reference frequency. The PLL cannot remain locked for all frequencies, and if the input reference frequency moves outside the *lock range*, (which is usually larger than the capture range), the PLL will drop out of lock.

Figure 2 illustrates the relationship between free-running frequency, capture range, and lock range.

TRANSIENTS AND PLLS:

The preceding analysis of PLL operation has described how the system acts under steady-state conditions (where the inputs are not changing and have not changed for a long period of time.) Because the VCO cannot change frequency instaneously, (it exhibits an effect very similar to the inertia of a rotating motor), and because negative feedback is present, the PLL's behavior under changing (dynamic) input conditions is described by a 2nd order differential equation. As you might expect, then, there is a loop *damping ratio* involved.

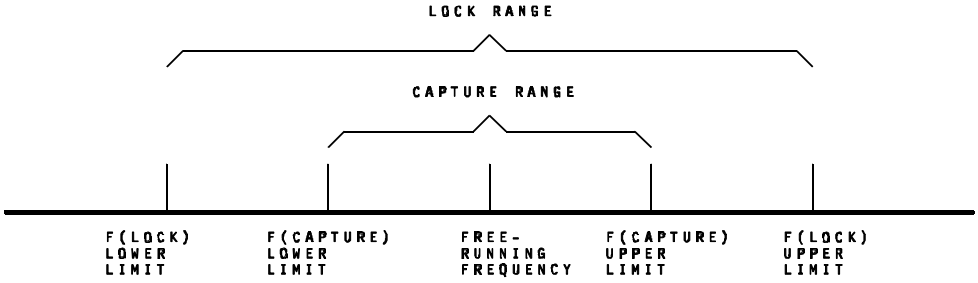

FIGURE 2: PLL OPERATING STATES

In most PLL designs, the damping ratio is set near 1/2. This means that faster response will occur to input transients (short-term changes) compared to a loop with a damping ratio of 1 or unity (critical damping), but a certain amount of loop "ringing" or "hunting" behavior will be present after each input change. *A designer controls damping ratio by controlling the loop natural frequency, and loop gain*. Simple component choices (typically outlined in data books) set these parameters. When designing a PLL, remember that the final stability of your circuit depends strongly on the damping ratio.

CIRCUIT ANALYSIS:

The PLL in this circuit is entirely contained within one IC chip, the Signetics NE-565.

All that we need to provide to build a complete, functioning PLL are timing elements (R_T, C_T) for the VCO, and a capacitor for the low-pass filter. (The NE-565 has a 3.6K resistor "on-chip" for the low-pass filter.)

In figure 3 (on the next page), the VCO timing is set by R_1, R_2, and C_2. The low-pass filter time-constant (which we will vary) is formed by the internal 3.6K resistor on pin 7, and C_5. The reference input goes to pin 2, one of the phase detector inputs. The other phase detector input on pin 5 is directly connected to the VCO output on pin 4, closing the loop.

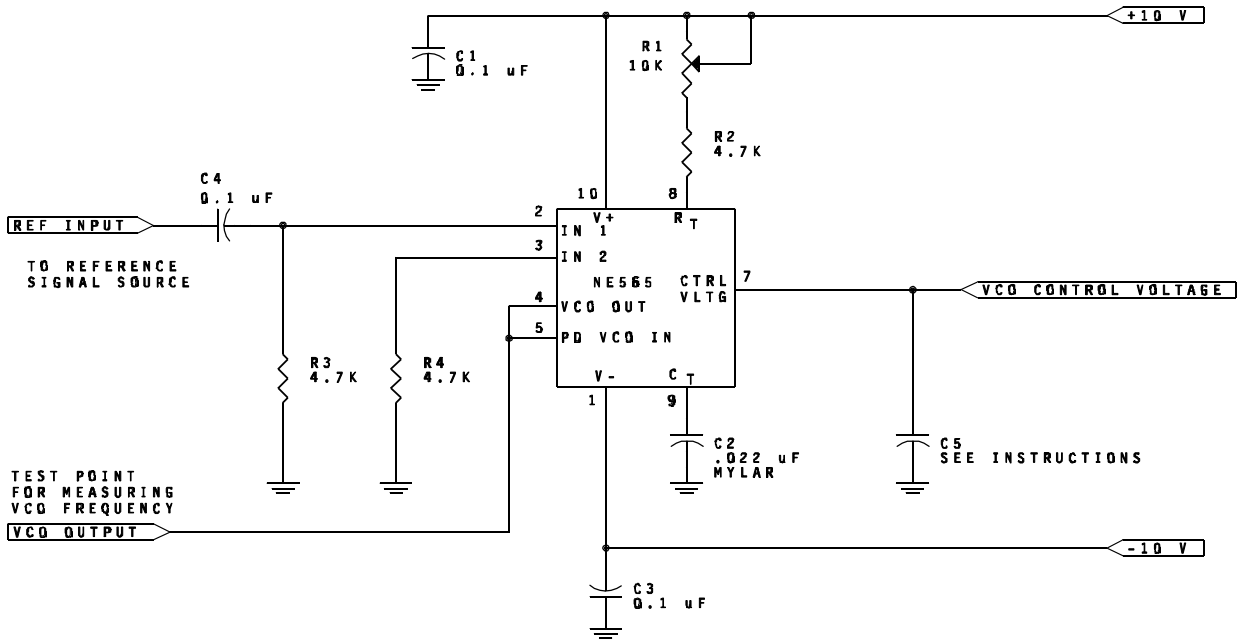

FIGURE 3: NE565 PLL EVALUATION CIRCUIT

LABORATORY PROCEDURE:

In this experiment, you will observe the operation of the PLL subsystem. You'll learn to recognize the three PLL states in actual circuits, and you will also gain some insight into how circuit values affect PLL operation.

YOU MUST USE A FREQUENCY COUNTER TO OBTAIN ACCURATE FREQUENCY READINGS. YOU WILL BE MEASURING THE *REFERENCE* INPUT FREQUENCY AND *VCO* OUTPUT FREQUENCY; MAKE SURE WHICH ONE IS BEING MEASURED -- IT MAKES A DIFFERENCE WHEN THE LOOP IS OUT OF LOCK!

1. Construct the circuit of Figure 3, using a 10 uF electrolytic for C_5. (C_5 is the capacitor for the loop low-pass filter.)

2. Apply power to the circuit, but don't apply a *reference* signal yet. We want to set the free-running frequency of the VCO. Adjust R_1 until the output frequency of the VCO on pin 4 is 1 KHz.

3. Apply the reference frequency to the *reference input* of the circuit.

4. Connect scope channel #1 to the reference input of the circuit, and scope channel #2 to the VCO output. Connect the frequency counter to the reference input, so that the frequency of the reference is displayed. (Be sure to trigger off channel #1, the reference input.)

5. Set the *reference* function generator to 600 Hz, approximately. Observe the two scope traces, and RECORD what you see. Does the loop appear to be in lock, or out-of-lock at this point? Why? (Provide this information in your report.)

6. Slowly increase the frequency of the generator until the PLL just locks. (The two traces will appear stable on the scope). A phase shift will be present between the VCO and reference frequency; this is OK. This frequency is the bottom of the *capture range*, F_c(min). Record it below.

   F_c(min) = _____

7. When the PLL is in lock, how do the outputs of the VCO and reference source compare? (Comment in your report.)

8. Let's find the top of the *lock range*. Slowly increase the frequency until the PLL again drops out of lock. This frequency is the top of the lock range, Flock(max). Record it below.

   F_{lock}(max) = _____

9. The PLL is now *out of lock*, and the reference frequency is above the top of the capture range. Slowly decrease the reference until the PLL locks again; this is F_c(max). Finally, decrease the reference frequency until the PLL drops out of lock again; this is F_{lock}(min). Record these values.

   F_c(max) = _____ F_{lock}(min) = _____

   With the four frequency measurements just made, you can now calculate the *capture* and *lock* ranges. The ranges are computed as follows:

   Capture_Range = F_c(max) - F_c(min)

   Lock_Range = F_{lock}(max) - F_{lock}(min)

   Do so, and record the values calculated.

10. Let's observe the output from the low-pass filter, to see what happens when the reference frequency is steady. We know it is supposed to be smooth DC, so we'll need to use the DC setting of the scope to see the DC component. We also know that no filter is perfect, so some AC ripple will be present on top of the DC. Set the reference frequency to 1 KHz, and record the oscilloscope reading of the low-pass filter output on pin 7 of the IC. Include this graph in your report. Don't forget to show both the DC and AC components.

11. The DC output from the low-pass filter should depend on the frequency of the *reference*. Record the DC output from the filter using a DMM for each frequency from 900 Hz to 1100 Hz, using 25 Hz intervals. RECORD this information in a data table, and produce a GRAPH of the data, titled "LOW PASS DC OUTPUT -VS- REFERENCE FREQUENCY."

12. The capture range depends on the low-pass filter of the PLL. Let's see how. Replace C_5 with each of the following values: 1 uF, 0.1 uF, .001 uF. Re-measure the capture and lock ranges for each capacitor value, and RECORD all results in a DATA TABLE in your report.

13. Describe the relationship you found between the capture range, and size of the filter capacitor in the low-pass filter. (Include in your conclusion.)

14. With the .001 uF capacitor in place, again set the reference frequency to 1 KHz, and record the low-pass filter output (as in step 10, include this graph in your report.)

15. How does the waveform in step 14 differ from that obtained in step 10, and why? (An examination of the values in the low-pass filter for the two steps may provide an answer.)