Phase Locked Loop Dynamics
and Practical Synthesizer Design

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Introduction

The phase-locked-loop, or PLL, finds wide application in communication systems. It is used primarily for frequency synthesis, but is also quite useful for modulation and detection of many forms of modulation, especially FM. This paper will concentrate on the practical application of the PLL as a frequency synthesizer; however, the derived relations can also be quite easily applied to other applications.

The Synthesizer Loop

Figure 1 shows the basic model for a direct PLL frequency synthesizer. The loop contains a *phase detector*, *low-pass filter*, *voltage-controlled-oscillator* or *VCO*, and an optional *divider*. The basic purpose of the PLL is to phase-lock the VCO onto the reference frequency (or a multiple thereof, dictated by the divisor block N).

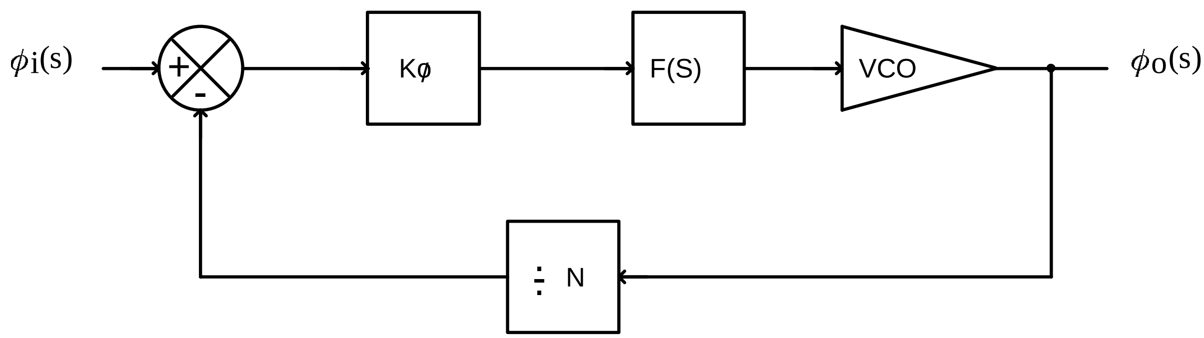

Figure 1: Phase Locked Loop Model

In normal operation, the phase detector outputs an error signal ε that is used to determine whether the VCO is leading or lagging the reference frequency. The error signal essentially points the VCO in the correct direction, and hopefully the VCO eventually locks onto the *exact* frequency desired. This frequency is predicted by the well-known equation:

(1) $f_{VCO} = N \ f_{ref}$

The output of a digital phase detector is a pulsating square-wave whose duty cycle is proportional to the phase difference between the reference input and the VCO. If this square-wave drives the VCO directly, the VCO frequency will rapidly jump between its minimum and maximum values as the phase-detector output pulses high and low.

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Obviously, this would generate significant and excessive FM sidebands in the synthesized output! In order to smooth the VCO control voltage, a low-pass filter is used.

The low-pass filter ideally extracts the DC component, leaving a nice smooth voltage to operate the VCO. However, the low-pass filter adds a pole to the PLL's transfer equation, which has a negative impact upon the loop stability. In general, the longer the RC time-constant of the filter, the slower the PLL will be to respond to an input change. Shorter RC time constants provide faster response times and higher spurious FM sideband levels.

Two types of filters are commonly employed in PLL work. Figure 2 illustrates a passive RC low-pass filter. Its primary advantage is simplicity and minimum component count. However, it is impossible to independently control the loop damping ratio and natural frequency with this filter, so it is seldom used except in simple design efforts.

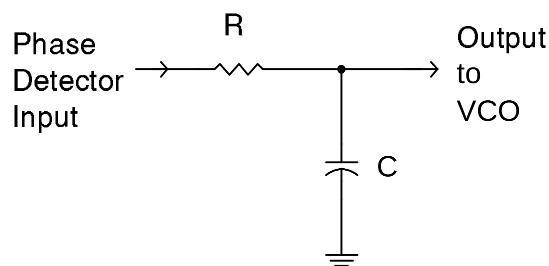

Figure 2: Passive Lag-Type Loop Filter

Figure 3 shows a typical active lead-lag RC integrator. The circuit has many advantages over the passive RC filter. First, loop damping ratio and damped natural frequency can be independently controlled using this filter. This is important in communications applications, since the ratio of reference frequency to loop damped natural frequency ω_d has a direct effect on suppression of undesired sideband energy (The higher the ratio, the better the suppression). Furthermore, the combination of loop damping ratio ζ and damped natural frequency ω_d directly control the loop *settling time*, which is defined as the time required for the output error to fall at or below a specified percentage of the final request value after a step input. Finally, an active RC filter can incorporate gain, and will be minimally affected by possible loading from the VCO control input.

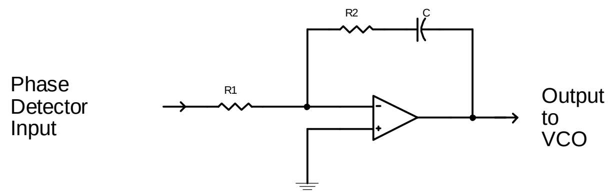

Figure 3: Active RC Lead-Lag Integrator

The passive RC filter approach is quite acceptable when it can meet design requirements; it only lacks in flexibility. The active filter is always easier to design; its primary disadvantage is the introduction of noise in its active element (operational amplifier).

The VCO is a critical block in the loop. *The closed-loop spectral purity can be no better than the open-loop spectral cleanliness of the VCO!* Therefore, special care must always be taken to ensure that the VCO can "meet specs." With the increasing emphasis on wideband operation in modern synthesizer design, this goal is becoming increasingly difficult to meet. (For many wideband designs, several VCOs are used -- one for each frequency range to be covered. Though costly, this method allows each VCO to be optimized for its frequency range.)

VCO outputs should always be buffered before driving a programmable divider to prevent digital switching transients from inadvertently frequency-modulating the VCO!

The *lock range* of a PLL is primarily determined by the phase-detector and VCO blocks. The lock range is simply the DC limit for oscillation frequency given the possible range of phase-detector error voltages.

The *capture range* of a PLL is more complex. It is approximated by computing the bandwidth of the closed-loop transfer equation.

The Synthesizer Loop Model

Figure 1 can be used to develop a mathematical model for the loop. In this model, the Laplace equivalent of each block will be used. In order to do this, two assumptions must be made. First, we must assume that the PLL is a *linear* system. This is largely true, and is highly dependent upon the linearity of the VCO and phase-detector blocks.

Second, we must also assume that the PLL remains in *lock*. When a PLL is out of lock, its behavior is highly non-linear, especially during capture.

The phase detector is modeled using two functional blocks, a summing junction and a gain block. The purpose of the phase detector is to generate an *error signal*, ε, which can be mathematically expressed as the difference of two input angles in 's':

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(2) $\varepsilon = K_\phi \{ \phi_i(s) - \phi_o(s) / N \}$

Where, ε = Phase detector output error signal;

K_ϕ = The conversion gain of the phase-detector, in Volts/radian;

$\phi_i(s)$ = The input "request" angle, which is really the integral of the reference frequency;

$\phi_o(s)$ = The VCO (Voltage Controlled Oscillator) output angle, which is the integral of the VCO output frequency;

N = The optional loop divisor. If there is no divider in the loop, N is equal to 1.

The low-pass filter smoothens the unfiltered DC error signal 'ε' in order to produce the output $V_c(s)$ for the VCO:

(3) $V_c(s) = \varepsilon\, F(s)$

Where F(s) = The transfer function of the low-pass filter, to be defined later in actual application.

The final output of the PLL is the VCO output frequency, $\omega(s)$. Because the VCO is a linear block, we can write:

(4) $\omega(s) = K_V\, V_c(s)$

Where K_V = The VCO conversion constant, in radian/S/Volt.

By combining the terms in equations (2) through (4), we get:

(5) $\omega(s) = K_\phi K_V F(s) \{ \phi_i(s) - \phi_o(s) / N \}$

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The output variable of equation (5) is not expressed appropriately for solving the closed-loop equation; the angle $\phi_o(s)$ is needed. This angle is derived by integrating $\omega(s)$:

$$(6) \qquad \phi_o(s) = \omega(s) / s$$

$$(7) \qquad \phi_o(s) = \frac{K_\phi K_V F(s)\{ \phi_i(s) - \phi_o(s) / N \}}{s}$$

Solving equation (7) for the ratio $\phi_o(s) / \phi_i(s)$ yields the fundamental transfer function of the phase locked loop system:

$$(8) \qquad \frac{\phi_o(s)}{\phi_i(s)} = \frac{K_\phi K_V F(s)}{s + K_\phi K_V F(s)/N}$$

Equation (8) reveals that the low-pass filter transfer function, F(s), determines much about the loop's dynamic behavior. It would be useful if this information were further generalized for filters that designers typically included in PLL designs.

Performance with the Active RC Integrator

Figure 3 illustrates the integrator circuit that will be used for this portion of the analysis. It is very typical of the circuit used in common practice. Most designers add components to the final circuit to improve FM sideband suppression as desired.

The loop performance with the filter of figure 3 is computed by writing the Laplace expression for the filter transfer function. For the active filter,

$$(9) \qquad F(s) = \frac{R_2Cs + 1}{R_1Cs} = \frac{R_2}{R_1} + \frac{1}{R_1Cs}$$

Although the single-fraction form of equation (9) is really an improper expression in s, it is more convenient for substitution into the loop transfer equation. Substituting equation (9) for F(s) in equation (8) yields:

$$(10) \qquad \frac{\phi_o(s)}{\phi_i(s)} = \frac{\{ K_\phi K_V(R_2Cs + 1) / R_1C \}}{s^2 + s\,(K_\phi K_V R_2 / NR_1) + (K_\phi K_V / NR_1C)}$$

The impulse response of the system can be computed by letting:

(11) $\phi_i(s) = \mathbf{L}\{\phi_i(t)\} = \mathbf{L}\{\delta(t)\} = 1$

The output response becomes:

(12) $$\phi_o(s) = \frac{\{K_\phi K_V(R_2Cs + 1) / R_1C\}}{s^2 + s(K_\phi K_V R_2 / NR_1) + (K_\phi K_V / NR_1C)}$$

The characteristic equation for a second-order system can now be applied to determine the response characteristics:

(13) $D(s) = s^2 + 2\omega_n\zeta s + \omega_n^2$

$D(s) = s^2 + s(K_\phi K_V R_2 / NR_1) + (K_\phi K_V / NR_1C)$

By rearranging the terms of equation (13), the following statements can be made:

(14) $\omega_n = (K_\phi K_V / NR_1C)^{1/2}$

Equation (14) gives the loop's *undamped natural frequency*. In practice, the loop will actually "ring" at a frequency lower than this called the *damped natural frequency*, ω_d. The only case in which the loop actually responds at this frequency (ω_n) is the marginally-stable case (undamped) where $\zeta = 0$. Note that the undamped natural frequency depends on the value of divisor N; this means that the designer should make sure that ω_n falls within acceptable design limits *over the entire desired range of divisors.*

The *damping ratio*, ζ, is actually the ratio of α/ω_n and is computed by:

(15) $\zeta = R2\ \sqrt{(K_\phi K_V C / 4NR_1)}$

Most designers start with an initial goal of $\zeta = 1/2$ to 3/4. A value of 1 for ζ represents *critical damping*. Critical damping produces the fastest possible response without oscillation.

The damped natural frequency represents the true resonant frequency of the loop, and is computed as:

(16) $\omega_d = \omega_n(1 - \zeta^2)^{1/2}$ For $0 <= \zeta < 1$

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The *settling time* is related to both the damping ratio, ζ, and the damped natural frequency ω_d. If $0 <= \zeta < 1$, which is usually the case, the impulse response will be a decaying sinusoid with the following characteristic equation:

$$\text{(17)} \quad \phi_o(t) = \frac{M}{\omega_d} \varepsilon^{-(\alpha t)} \sin(\omega_d t + \theta)$$

The damping constant, α, can be expressed as $\zeta\omega_n$ in equation (17). Therefore, the settling time to a given percentage γ can be easily approximated by solving for the point in time that equation (17) becomes equal to the quantity $\gamma\{M/\omega_d\}$:

$$\text{(18)} \quad t_s = \frac{-\ln\gamma}{\zeta\omega_n}$$

Note that equation (18) reveals an important relationship between the loop natural frequency, ω_n, and loop settling time*: Increasing the natural frequency decreases the loop settling time*. However, there is a hidden penalty for increasing ω_n: Decreased reference frequency sideband suppression. Therefore, there is a trade-off between these two parameters in practical designs. For reasonable suppression of reference frequency sidebands, most designers force ω_n to be 1/50 or 1/100 of the reference frequency.

For this circuit configuration, the product $\zeta\omega_n$ can be found more directly by combining equations (14) and (15), which produces a much simpler expression for t_s:

$$\text{(19)} \quad \alpha = \zeta\omega_n = R_2 \sqrt{(K_\phi K_V C / 4NR_1)} * \sqrt{(K_\phi K_V / NR_1 C)}$$

$$\text{(20)} \quad \alpha = (K_\phi K_V R_2 / 2NR_1)$$

$$\text{(21)} \quad t_s = \frac{-2 N R_1 \ln\gamma}{K_\phi K_V R_2}$$

Design Procedure: Active RC Integrator

There are two primary design objectives in the design of direct PLL synthesizers:

A. Design objective: Loop Settling Time
B. Design objective: Minimum spurious sidebands from the reference frequency.

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As seen in the previous analysis, these two goals are mutually exclusive. A gain in one area causes a loss in the other. There are advanced techniques for optimizing both, such as adaptive filtering (under software control), but they are beyond the scope of this paper. The goal of minimum spurious sideband content will therefore be pursued. The designer must judge if the results are appropriate, and if not, make changes as needed.

Basic Design Steps - Direct Synthesizer, Active Filter, Minimum Spurious Emissions

1. Choose f_{ref}, R_1, K_ϕ, N_{min}, N_{max}, K_V, and ζ_{mid}.

a. R_1 will normally be between 2K and 47K Ohms.
b. It is suggested to start with ζ_{mid} = 1/2 to 3/4.
c. K_ϕ and K_V must be measured from the actual circuit, or be computable.
d. f_{ref} is the PLL reference frequency, nominally equal to the frequency steps.

2. Use N_{mid} for basic loop calculations to follow:

(22) $$N_{mid} = (N_{min} + N_{max}) / 2$$

3. Set the loop natural frequency, ω_n, 50 to 100 times below the reference frequency. This is fairly-well accepted design practice, and helps to suppress the reference frequency from appearing in the loop output:

(23) $$\omega_{ref} = 2 \pi f_{ref}$$

(24) $$\omega_n = \omega_{ref} / 100$$ *You may use 50 to 100 for a starting point.*

4. The combination of R_1 (already chosen) and C will now set ω_n as desired. As derived from equation (14), C is now computed:

(25) $$C = \frac{K_\phi K_V}{N_{mid} R_1 \omega_n^2}$$

Note: If a suitable value for C is not available, try adjusting R_1 and repeating this step.

5. Now set the loop damping ratio ζ_{mid}. This is adjusted by setting the value of R_2 as derived from equation (15):

(26) $$R_2 = \frac{\zeta_{mid}}{\quad}$$

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$\sqrt{(K_\phi K_V C / 4N_{mid}R_1)}$

6. Using equations (14), (15), and (21), verify the loop performance characteristics:

   a. These characteristics should be evaluated for the entire divisor range N, from N_{min} to N_{max}.

   b. Equation (21) gives the approximate loop settling time. You must choose a value for gamma (γ). Most designers choose 10%.

6. Note that <u>lock range is not a part of the design calculation</u>. Using the active-integrator approach gives a DC loop gain of *infinity*, almost eliminating this issue. The designer must only make sure that the amplifier has sufficient compliance (peak-to-peak output swing) to produce the required range of VCO control voltages. *For practical operational amplifiers, this means that the power supply rail voltage for the op-amp needs to be high enough to obtain the maximum anticipated control voltage at the op-amp output pin without causing the amplifier to saturate*.

IMPORTANT: Make absolutely sure that the operational amplifier can handle the signal bandwidths expected in the filter circuit. Insufficient amplifier bandwidth will cause severe changes in loop performance and stability. This is especially important for high reference frequencies (10 Khz and above).

7. Construct a prototype, and verify that specifications are made.

   a. Many designers make the following modifications to the active integrator in order to increase reference rejection. The relations for these added components will be stated, but not derived.

   b. In adding additional components to the loop, ensure that sufficient *phase margin* remains over the entire divisor range. Phase margins less than 30^o are marginal and may lead to loop oscillation!

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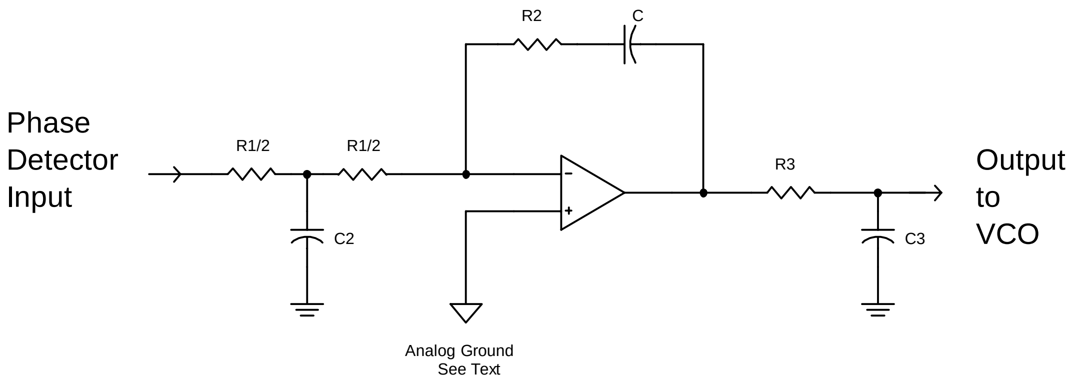

Figure 4: Modified Active Integrator

c. In the modified circuit, R_1 is split into two equal parts. The capacitor C_2 is then calculated by:

(27) $$C_2 = \frac{\pi}{10 R_1 \omega_n}$$ The pole from R_1's halves and C_2 is at 12 ω_n.

d. R_3 and C_3 are optional and can provide extra suppression. Their absolute values are not important, as long as their impedance is small when compared to the input impedance of the VCO. The pole due to R_3 and C_3 should be placed at 15 or 16 ω_n as follows:

(28) $$15\,\omega_n = \frac{1}{R_3 C_3}$$

Important: "Analog Ground" is the mid-point bias potential for the op-amp. For phase detectors operating from 5V, this point should be biased to 2.5V DC. Alternatively, use of differential phase detector outputs (where available) eliminates this issue.

Design Example

A direct PLL synthesizer was designed according to the following specifications:

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1. f_{out} = 27.500 Mhz to 29.999 Mhz in 1 Khz steps.
2. Available VCC = 12V regulated.
3. PLL frequency selection to be made by microprocessor program.
4. Settling time to 10% to be less than 100 mS.
5. Unwanted sideband suppression better than 60 dB

Design Steps

1. f_{ref} = 1 Khz to achieve 1 Khz frequency steps.

   R_1 = 15 K by arbitrary choice.

   A Motorola MC145170 single-chip PLL is to be employed with V_{DD}=5V. The phase detector gain K_ϕ therefore is $V_{DD}/4\pi$ = 0.3979.

   A Colpitts oscillator using an NPN transistor was designed for the synthesizer. The oscillator is modulated using varactor diodes, and has a frequency range of 27 to 31 Mhz, which is more than adequate to ensure sufficient lock range for the PLL. The measured sensitivity of the oscillator was K_V = 4.1524×10^6 Volt/Rad/Sec.

2. The average divisor value $N_{mid} = (N_{min} + N_{max}) / 2$ = (27,500 + 29,999) / 2 = 27,749. 5. The fractional remainder is ignored giving N_{mid} = 27,749.

3. The natural frequency ω_n is to be 100 times below the reference frequency ω_{ref}:

   $\omega_{ref} = 2\pi fref = 6283$ r/s

   $\omega_n = \omega_{ref} / 100 = 62.83$ r/s (About 10 Hz).

4. From equation (25), the capacitor can now be computed:

$$C = \frac{K_\phi K_V}{N_{mid} R_1 \omega_n^2} = \underline{1.0055\ \mu F}$$

Note: *The capacitor in the filter must be non-polarized*. Electrolytic capacitors should be avoided due to their poor tolerance and temperature sensitivity. Two 0.47 μF mylar capacitors have been used in the filter circuit for this reason.

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5. R_2 was calculated using equation (26). ζ_{mid} was set to <u>1/2</u> to decrease the loop bandwidth, and hence increase unwanted sideband suppression:

$$R_2 = \frac{\zeta_{mid}}{\sqrt{(K_\phi K_V C / \ 4N_{mid}R_1)}} = \underline{15.872\ K}\ \text{(16 K standard)}$$

The sideband suppression due purely to the loop bandwidth can be *estimated* using the following relation:

(29) $dB_{supp} \approx 20 \log_{10} (\omega_{ref} / \omega_{3dB})$

Where $\omega_{3dB} = \omega_n \sqrt{\{ 2\zeta^2 + 1 + \sqrt{[(2\zeta^2 + 1)^2 + 1]} + 1 \}} = 114$ r/s

The suppression is $20 \log_{10} (6283 / 114) =$ <u>34.8 dB</u> with $\zeta = 1/2$. This is clearly inadequate performance, therefore additional measures must be taken to improve suppression.

6. For additional sideband suppression, both optional networks specified earlier were added. R_1 therefore becomes R_{1a} and R_{1b}, <u>two 7.5 K resistors</u>. The capacitor C_2 was calculated according to equation (27):

$$C_2 = \frac{\pi}{10R_1\omega_n} = \underline{0.333\ \mu F}\ \text{(0.33 }\mu\text{F standard)}$$

This measure adds to the suppression performance. The added suppression can be estimated by using equation (29):

$$dB_{supp} \approx 20 \log_{10} (\omega_{ref} / \omega_{3dB})$$

The pole of the filter formed by R_{1a}, R_{1b}, and C_2 is at:

$\omega_{3dB} = 4/(R_1C_2) = 808$ r/s (Note, $R_1 = R_{1a} + R_{1b}$)

The additional suppression is:

$$dB_{supp} \approx 20 \log_{10} (6283 / 808) \approx \underline{17.82\ dB}$$

The total suppression would now be 17.82 dB + 34.8 dB ≈ 52.6 dB.
<u>This is still inadequate</u>, so additional filtering will be employed.

For the second optional network, R3 was chosen as 10K (the VCO input impedance was estimated at 100K or larger). Using equation (28):

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$$C_3 = \frac{1}{R_3 15\,\omega_n} = 0.10611\,\mu f \quad (\,0.1\,\mu F \text{ standard})$$

The suppression due to C_3 and R_3 is now added to the total:

$$\omega_{3dB} = 1 / C_3\, R_3 = 1000 \text{ r/s}$$

$$dB_{supp} \approx 20 \log_{10} (\,\omega_{ref} / \omega_{3dB}\,) \approx 20 \log_{10} (\,6283 / 1000\,) \approx \underline{15.9 \text{ dB}}$$

The total suppression is now 17.82 dB + 34.8 dB + 15.9 dB ≈ <u>68.6 dB</u>

Because these relationships are only approximations, measurements must be made with an actual prototype in order to confirm the spectral performance. The equations assume perfect VCO characteristics, and zero loop noise. Actual performance will probably be at least 3 dB worse than the estimate.

7. The synthesizer settling time can be verified using equation (21):

$$t_S = \frac{-\,2\,N\,R_1 \ln\gamma}{K_\phi K_V\,R_2} = \underline{78.4 \text{ mS}} \text{ @ } N_{max} \text{ and } \gamma = .1, \text{ which meets specs.}$$

8. Phase margin should be evaluated to ensure that the loop remains stable over the entire divisor range. The loop employs negative-feedback, so the initial loop phase shift is 180^o. The *integrating effect* of the VCO (1/s) adds another 90^o of initial shift. If enough phase lag is present to give a 360^o phase shift (or 0^o phase shift), the loop will break into oscillation. Phase margin will in general be worse as ω_n increases, since the loop filter configuration produces phase lag. Therefore, phase margin will be evaluated for maximum ω_n which occurs at N_{min} according to equation (14):

$$\omega_n = (\,K_\phi K_V / \; NR_1C\,)^{1/2}$$

$$\omega_n = 63.28 \text{ r/s} \qquad \text{(Maximum value when N=27,500)}$$

There are three poles in the filter network. The first one is in the active integrator. Equation (9) gives the transfer equation of this circuit:

$$(9) \qquad F(s) = \frac{R_2Cs + 1}{R_1Cs} = \frac{R_2}{R_1} + \frac{1}{R_1Cs}$$

By letting s = jw, we can write the expression for $A_v \angle \theta$:

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(30) $A_v \angle \theta = \sqrt{\ \{ (R_2 / R_1)^2 + (1 / j\omega R_1 C)^2 \}} \angle \tan^{-1} (-1 / \omega R_2 C)$

At the natural frequency of 63.28 r/s, the phase shift in the integrator is:

$\theta = \tan^{-1} (-1 / \omega R_2 C) = \underline{-44.6^o}$

The remaining phase margin is $90^o + (-44.6^o) = \underline{45.4^o}$
There is plenty of phase margin left so far.

The second pole is in the added filter from splitting R_1 in half and adding C_2. Assuming that the phase detector output impedance is much smaller than R_1, the Thevenin resistance seen by C_2 is really R_1 / 4. Therefore:

(31) $\theta = \tan^{-1} (R_{th} / Xc) = \tan^{-1} (-\omega R_1 C_2 / 4) = - 4.5^o$

The remaining phase margin is now $135.36^o + (-4.5^o) = \underline{40.9^o}$
Finally, components R_3 and C_3 add the third pole. The added angle due to this pole is thus calculated:

$\theta = \tan^{-1} (R_{th} / Xc) = \tan^{-1} (-\omega R_3 C_3) = - 3.6^o$

The final and total phase margin is $130.9^o + (-3.6^o) = \underline{37.3^o}$.

The loop stability has been verified, since there is insufficient phase shift, even with maximum loop gain (N minimum) to cause oscillation. Most designers consider phase margins less than 30 degrees to be potentially unstable, considering component value variations.

9. Figure 5 shows the completed synthesizer. For testing, the following data was programmed into the MC145170 registers:

CONFIG = \$E3	(Chip configuration register)
R = \$27B0	(Reference divisor used a 10.160 Mhz crystal)
N = \$6B6C to \$752F	(Programmable divider test, 27.500 Mhz to

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29.999 MHz)

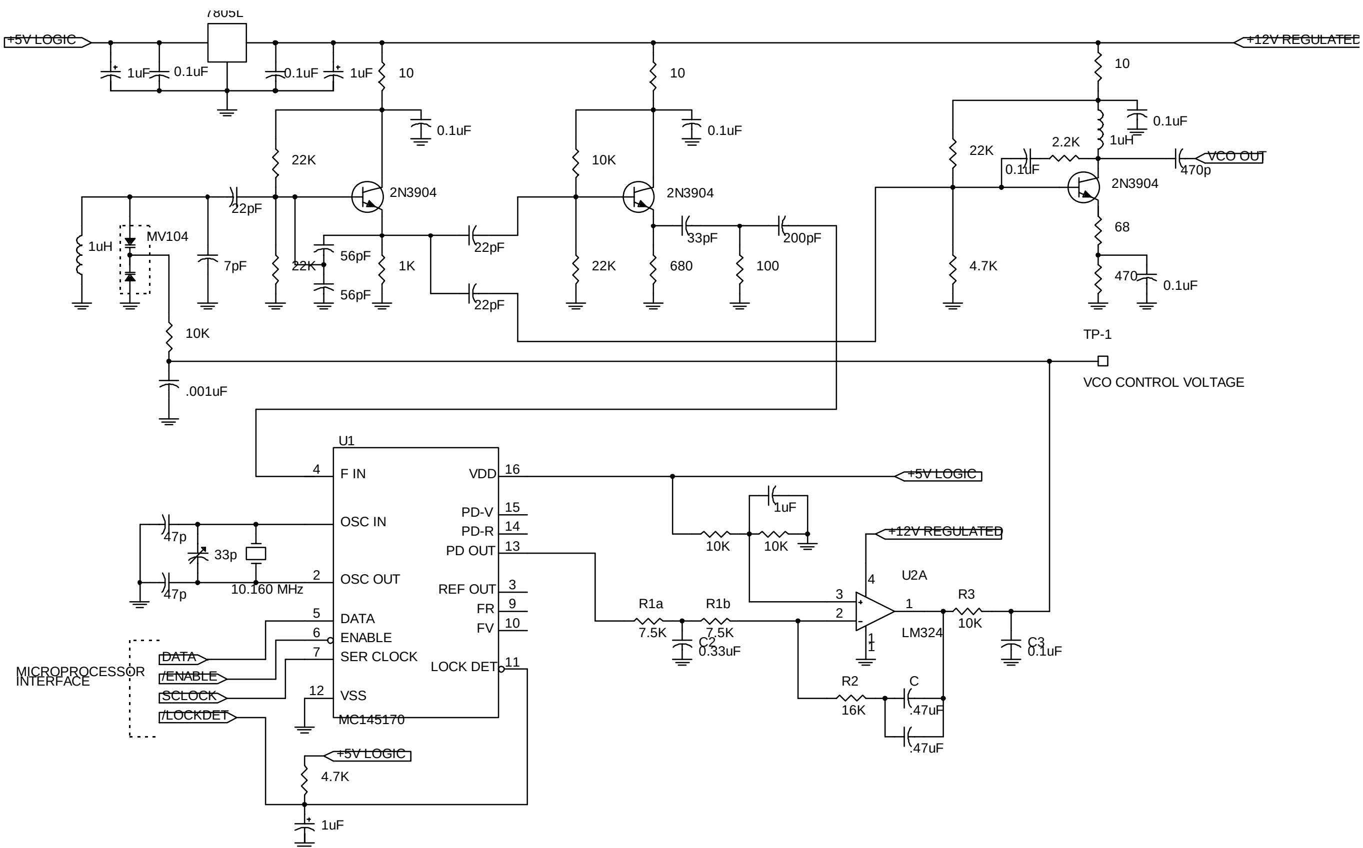

Figure 5: Complete 10-Meter Synthesizer

Performance with a Passive RC low-pass filter

Figure 2 shows the schematic of a simple low-pass filter employing one capacitor and one resistor. The circuit is temptingly simple, but has several important drawbacks that limit its use. These limitations will become apparent with further examination.

The transfer function of the filter of figure 2 can be written as:

$$(32) \qquad F(s) = \frac{1}{1 + sRC}$$

Substitution of equation (32) into equation (8) yields:

$$(33) \qquad \frac{\phi_O(s)}{} = \frac{\{ K_\phi K_V / RC \}}{}$$

$$\phi_i(s) \qquad s^2 + s/RC + \{K_\phi K_V / NRC\}$$

The impulse response of the system can be computed by again letting:

(34) $\phi_i(s) = \mathbf{L}\{\phi_i(t)\} = \mathbf{L}\{\delta(t)\} = 1$

The output response of the system for the impulse is:

(35) $$\phi_o(s) = \frac{\{K_\phi K_V / RC\}}{s^2 + s/RC + \{K_\phi K_V / NRC\}}$$

The characteristic equation for a second-order system can now be applied to determine the response characteristics:

(36) $D(s) = s^2 + 2\omega_n \zeta s + \omega_n^2$

$D(s) = s^2 + s/RC + \{K_\phi K_V / NRC\}$

By rearranging the terms of equation (36), the loop parameters can be expressed in terms of the circuit element values:

(37) $\omega_n = (K_\phi K_V / NRC)^{1/2}$

(38) $\zeta = (N / 4RCK_\phi K_V)^{1/2}$

(39) $\omega_d = \omega_n (1-\zeta^2)^{1/2}$ For $0 <= \zeta < 1$

The settling time can be *estimated* by:

(18) $$t_s = \frac{-\ln\gamma}{\zeta\omega_n}$$

For this circuit configuration, the product $\zeta\omega_n$ can be found more directly by combining equations (37) and (38), which produces a much simpler expression for t_s:

(39) $$t_s = \frac{-\ln\gamma}{1/(2RC)} = -2RC\ln\gamma$$

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Design Procedure: Passive RC Low-Pass Filter

As seen in the previous analysis, *reference frequency rejection* and *settling time* are common issues of interest to synthesizer designers. With the passive RC filter, these design choices are quite limited, and often the desired specifications will not be within the design envelope of this filter, in which case a more complex filter should be adopted.

Basic Design Steps

1. Find the values of N_{mid}, K_ϕ, K_v.

2. Choose the desired values for ζ and C.

3. Compute the resistor R for the filter:

$$(40) \qquad R = \frac{N_{mid}}{4\zeta^2 C\, K_\phi\, K_v}$$

4. *Evaluate* the parameters ω_n and ω_d. These parameters can *not* be independently controlled with respect to ζ with this filter configuration.

$$(37) \qquad \omega_n = \left(K_\phi K_V / \; NRC \right)^{1/2}$$

$$(39) \qquad \omega_d = \omega_n \left(1 - \zeta^2 \right)^{1/2}$$

5. If the value of ω_n is not suitable, try a different value for ζ and return to step 3. If suitable ω_n is not attainable, try a different filter design (active.)

6. The settling time of the loop can be evaluated using equation (39):

$$(39) \qquad t_S = -\,2RC \ln \gamma$$

Where γ is the percentage of settling; usually 1 to 10%.

Design Example

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A direct PLL synthesizer is to be designed to the following specifications using a passive LP filter. The specifications are very similar to the synthesizer in the previous example for the purpose of comparison.

1. f_{out} = 27.500 Mhz to 29.999 Mhz in 1 Khz steps.
2. Available VCC = 12V regulated.
3. PLL frequency selection to be made by microprocessor program.
4. Settling time to 10% to be less than 100 mS.
5. Unwanted sideband suppression better than 60 dB

Design Steps

1. Find the values of N_{mid}, K_ϕ, K_v.

Because the passive LP filter provides no voltage gain, a stage with a DC voltage gain of 2 V/V is necessary between the low-pass filter and VCO if the previous VCO design is used. This increases the effective conversion constant K_ϕ of the VCO to <u>8.8305 x 10^6 rad/sec/volt</u>.

As before, N_{mid}= <u>28749</u> and K_ϕ = <u>0.3979 volt/rad</u>.

2. Choose the desired values for ζ and C.

A good starting point is ζ = 1/2 and C=0.47 μF. The capacitor is an arbitrary choice.

3. Compute the resistor R for the filter:

$$R = \frac{N_{mid}}{4\zeta^2 C\, K_\phi\, K_v} = \underline{17.408\ K}$$

4. *Evaluate* the parameters ω_n and ω_d.

$$\omega_n = \left(K_\phi K_V / \ NRC \right)^{1/2} = \underline{122.22\ r/s}$$

Note that reference frequency suppression will be worse with this filter, because the loop natural frequency is higher. Increasing R will lower the natural frequency at the expense of lowering ζ and increasing settling time.

Additional filtering will have to be applied to meet the spurious emission specifications.

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6. The settling time of the loop can be evaluated using equation (39):

$$t_S \approx -2RC \ln \gamma = -2RC \ln 0.1 \approx \underline{37.6\text{ mS}}.$$

The settling time meets specification; in fact, the low value suggests that increasing the RC time constant would be a good design move.

Increasing R to 43K (Std) will increase the settling time to 93 mS, and reduce the natural frequency ω_n to 77.7 r/s, which will improve reference frequency rejection.

Conclusions

The two approaches to direct synthesizer design shown in this paper clearly demonstrate that trial-and-error methods are totally unnecessary in PLL work. The methods presented in this work will provide the engineer with results that work just as well in the real world as on paper. The designs given are intended only as starting points.

Successful synthesizer design requires expertise in several specialties, notably oscillator design, RF amplifier design, analog interfacing and noise/interference reduction techniques, as well as microprocessors. The range of skills required is most likely to be satisfied by using a team approach to design.

For DeVry Students:

The program "plldes.exe" in the *EET368 software archive* will perform the calculations for the active filters described in this paper. You may wish to download this program and let it walk the calculations in the design example given.

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