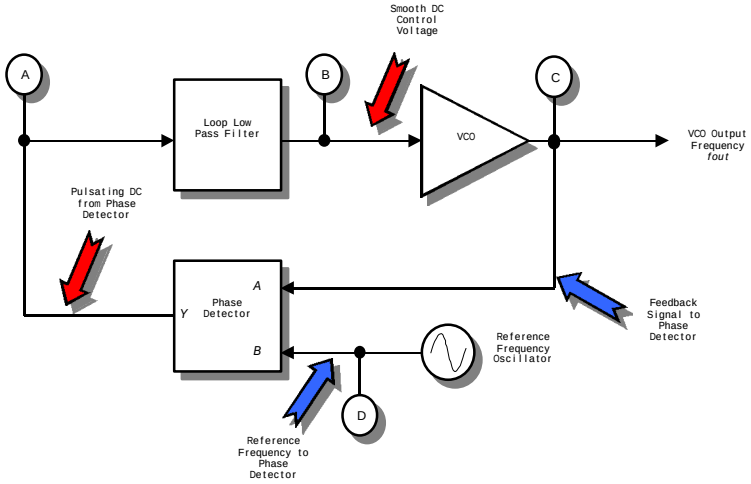
Homework #7 Solution Set

(10 points - 1 per problem)

1. *What is a frequency synthesizer? When is crystal control of an oscillator's frequency inadequate*?

   A frequency synthesizer is a circuit that *synthesizes* or "builds" new frequencies. These new frequencies are based on a highly stable frequency source, which is usually a single quartz crystal oscillator.

2. *Draw a block diagram of a phase locked loop. At each major test point, describe the function and nature of the signal (digital, analog, AC, DC, etc.)*



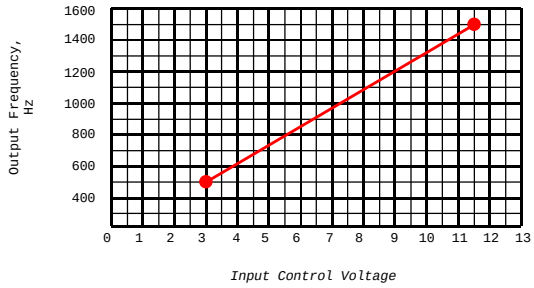
[Figure 7-1]

Test point A: Pulsating DC output from phase detector
Test point B: Smooth DC control voltage for VCO
Test point C: VCO Frequency output (frequency matches reference signal)
Test point D: Reference frequency input (steady AC frequency)

3. *If a frequency of 1.2 KHz is present at point D in figure 7-1, what frequency should be present at point C, and why*?

   Test point C should also have a frequency of 1.2 KHz due to the self-correcting action of the PLL.

4. *If 1.2 KHz is present at point D in figure 7-1, and the VCO has the transfer characteristic indicated in figure 7-2, what DC voltage will appear at point B*?



[Figure 7-2]

Point B should have a DC voltage of 9 Volts, as that is the potential necessary to get the VCO to operate at 1.2 KHz.

5. *If the frequency at test point D in figure 7-1 is increased from 1.22 KHz to 1.3 KHz, explain what will happen to the DC voltage at point B in the loop. Assume the VCO transfer characteristic of figure 7-2.*

As the frequency at test point D is increased, the VCO frequency will increase due to the closed-loop action of the PLL. Thererefore, the DC voltage at test point B will increase to approximately 9.8 Volts.

6. *State Finley's Law for phase detectors. How does a phase detector achieve "zero frequency error?*"

If the two inputs of a phase detector are not at exactly the same frequency, then the phase detector output will be in either positive or negative saturation.

Zero frequency error is produced because the phase detector compares *phase*, not frequency. As long as two signals have a constant phase difference (phase error), they will always be at the same exact frequency.

7. *What is the shape of the signal from a phase detector? What loop element smoothes this signal prior to driving the VCO*?

The signal from the phase detector is a square wave or pulse waveform. The low pass filter is responsible for smoothing this signal prior to its application to the VCO control input.

8. *List the three possible operating states of a PLL, and for each one, give the input conditions necessary to attain that state.*

a) Free Running: No input signal applied to the reference input.
b) Capture: Signal just applied to the reference input, but insufficient time elapsed to allow the loop to lock.
c) Locked: Loop has acquired input signal, and $f_{vco} = f_{reference}$.

9. *Which PLL components primarily determine the (a) Lock range, and (b) Capture range*?

   a) The lock range is primarily controlled by the VCO.
   b) The capture range is determined by the loop low-pass filter.

10. *Explain where a dual-trace oscilloscope is connected in a PLL to determine its operating condition (locked or unlocked).*

    A dual-trace oscilloscope should have one channel connected to the reference input, and the other channel connected to the VCO output. Alternatively, the scope channels can be connected to both inputs of the phase detector, which for simple PLLs is the same as the previously-mentioned outputs.