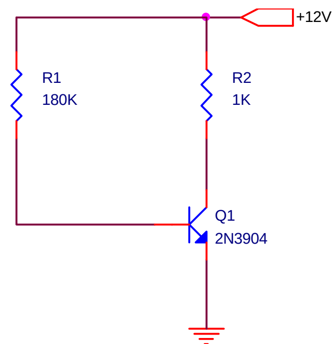
EET-225 Homework #4
Sr. Professor Wheeler

<u>Instructions</u>: This homework must be turned in within a flat 3-tab paper folder (no three-ring binders will be accepted). Answers must be written very neatly or typed. Use complete sentences when answering all questions. Where a problem involves a circuit, you must redraw the circuit as part of the solution, showing all indicated voltages and currents on the circuit diagram. Box or underline all final answers and show all work (see syllabus for example of homework standards).

1. Calculate the collector current and Gamma (γ) of the circuit below for β_{DC} = 100 and 150. Draw the load line, showing the Q-point of the circuit.



The collector saturation current is:

$$I_{C(SAT)} = \frac{V_{CC}}{R_C + R_E} = \frac{12V}{1K + 0} = 12mA$$ (This defines one end of the load line)

The cutoff voltage $V_{CE(OFF)}$ is V_{CC} (12V) (This defines the other end of the load line)

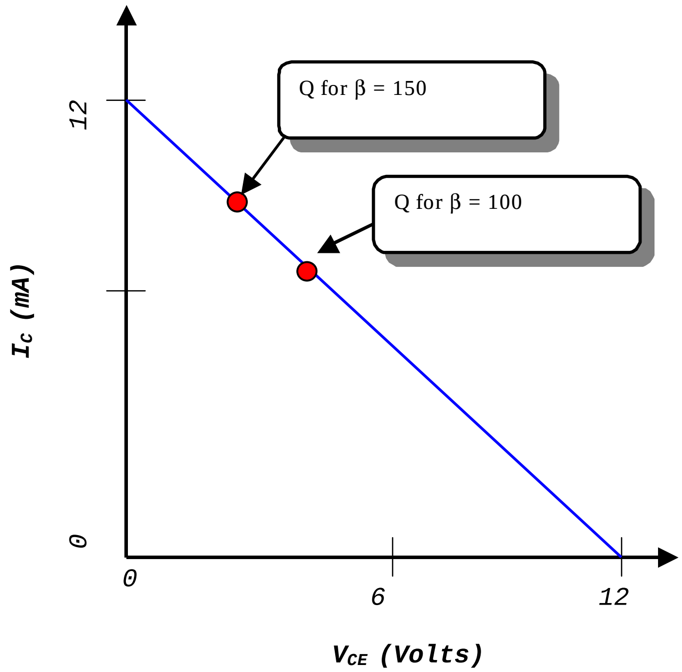
When β_{DC} = 100, the collector current can be calculated by:

$$I_C = bI_B = b\left(\frac{V_{CC} - V_{BE}}{R_B}\right) = (100)\left(\frac{12V - 0.7V}{180K}\right) = \underline{\underline{6.27mA}}$$

When β_{DC} = 150, the collector current becomes:

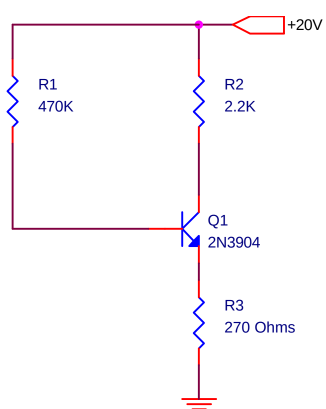
$$I_C = bI_B = b\left(\frac{V_{CC} - V_{BE}}{R_B}\right) = (150)\left(\frac{12V - 0.7V}{180K}\right) = \underline{\underline{9.42mA}}$$

The resulting load line looks like this:



The Q-point isn't very stable with base bias; the collector current directly depends upon β_{DC}, which isn't very desirable.

2. Calculate the collector current and Gamma (γ) of the circuit below for β_{DC} = 100 and 200. Draw the load line, showing the Q-point of the circuit.



The collector saturation current is:

$$I_{C(SAT)} = \frac{V_{CC}}{R_C + R_E} = \frac{20V}{2.2K + 270\Omega} = 8.09mA$$ (This defines one end of the load line)

The cutoff voltage $V_{CE(OFF)}$ is V_{CC} (20V) (This defines the other end of the load line)

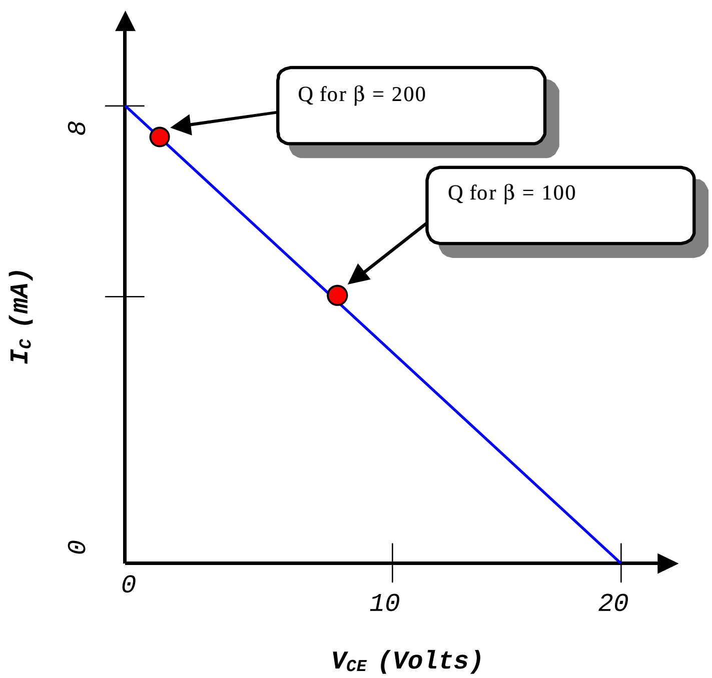
When β_{DC} = 100, the collector current can be calculated by:

$$I_C = \frac{V_{CC} - V_{BE}}{R_E + R_B / b_{DC}} = \frac{20V - 0.7V}{270\Omega + 470K / 100} = \underline{\underline{3.88mA}}$$

When β_{DC} = 200, the collector current becomes:

$$I_C = \frac{V_{CC} - V_{BE}}{R_E + R_B / b_{DC}} = \frac{20V - 0.7V}{270\Omega + 470K / 200} = \underline{\underline{7.36mA}}$$

The load line looks like this:



The overall bias is still not as stable as we can make it, however it is slightly better than base bias.

3. Design an emitter-feedback bias circuit to meet the following specifications:

Rc = 4.7 K $\quad\quad$ γ = 0.5 $\quad\quad$ Vcc = 20 V

β_{DC} = 100 to 200 (use geometric average)

Show all calculations and neatly draw the resulting circuit configuration.

Design steps:

1) $V_{CE} = gV_{CC} = (0.5)(20V) = 10V$

2) $V_E = 1V$

3) $V_C = V_E + V_{CE} = 1V + 10V = 11V$

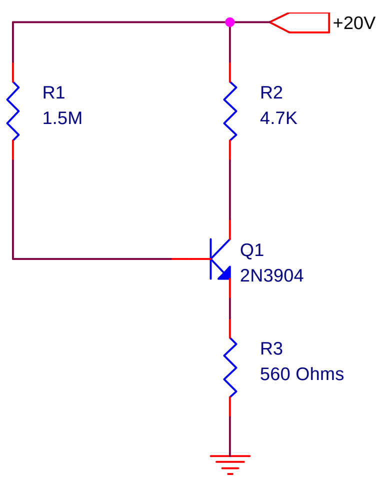
4) $I_E \approx I_C = \frac{V_{CC} - V_C}{R_C} = \frac{20V - 11V}{4.7K} = 1.91mA$

5) $R_E = \frac{V_E}{I_E} = \frac{1V}{1.91mA} = 522.2\Omega$ (560 Ω standard)

6) $\hat{b} = \sqrt{b_{MIN} b_{MAX}} = \sqrt{(100)(200)} = 141$

$R_B = \frac{V_{CC} - V_B}{I_E / \hat{b}_{DC}} = \frac{20V - (1V + 0.7V)}{1.91mA/141} = 1.348M\Omega$ (1.5 MΩ standard)

The circuit looks like this:



4. Design an emitter-feedback bias circuit to meet the following specifications:

Rc = 2.2 K γ = 0.3 Vcc = 30 V
β_{DC} = 150 to 300 (use geometric average)

Show all calculations and neatly draw the resulting circuit configuration.

Design steps:

1) $V_{CE} = gV_{CC} = (0.3)(30V) = 9V$

2) $V_E = 1V$

3) $V_C = V_E + V_{CE} = 1V + 9V = 10V$

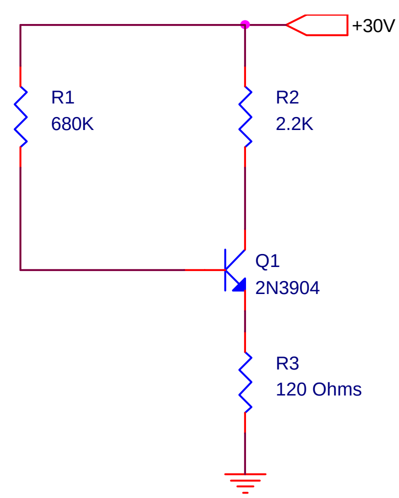
4) $I_E \approx I_C = \dfrac{V_{CC} - V_C}{R_C} = \dfrac{30V - 10V}{2.2K} = 9.09mA$

5) $R_E = \dfrac{V_E}{I_E} = \dfrac{1V}{9.09mA} = 110\Omega$ (120 Ω standard) (Note: 100 Ω is equally close)

6) $\hat{b} = \sqrt{b_{MIN} b_{MAX}} = \sqrt{(150)(300)} = 212$

$R_B = \dfrac{V_{CC} - V_B}{I_E / \hat{b}_{DC}} = \dfrac{30V - (1V + 0.7V)}{9.09mA/212} = 659.956K\Omega$ (680KΩ standard)

The circuit looks like this:



5. Design a collector-feedback bias circuit to meet the following specifications:

Rc = 1 K γ = 0.5 Vcc = 10 V
β_{DC} = 150 to 250 (use geometric average)

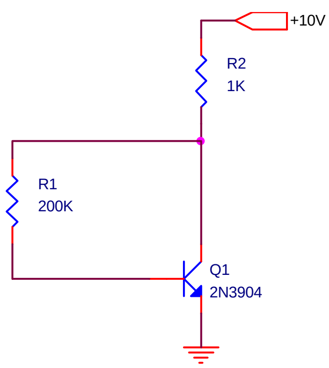
Show all calculations and neatly draw the resulting circuit configuration. Verify the design using any method of your choice and document your results.

Design steps:

1) $\hat{b} = \sqrt{b_{MIN} b_{MAX}} = \sqrt{(150)(250)} = 193.7$

2) $R_B = \hat{b} R_C = (193.7)(1K) = 193.7K$ ($\underline{\underline{200K}}$ standard)

Circuit configuation:



Verification of design:

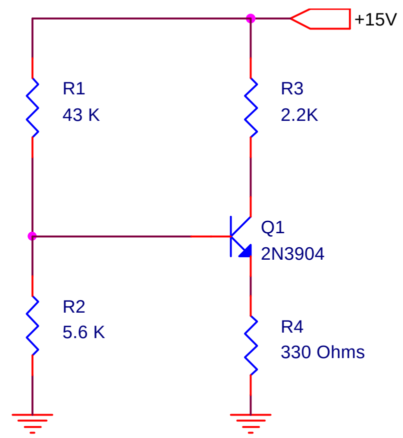
$$I_C = \frac{V_{CC} - V_{BE}}{R_C + R_B / b_{DC}} = \frac{10V - 0.7V}{1K + 200K/193.7} = 4.57mA$$

$$V_{CE} = V_C = V_{CC} - I_C R_C = 10V - (4.57mA)(1K) = 5.42V$$

$$g = \frac{V_{CE}}{V_{CC}} = \frac{5.42V}{10V} = \underline{\underline{0.542}}$$

(This verifies the proper placement of the Q-point, which was specified as 0.5)

6. Calculate the collector current and Gamma (γ) for the circuit below for β_{DC} = 100 and 200. Draw the load line, showing the Q-point of the circuit. Comment on the circuit's stability; how does it compare with the circuits from problems 1 and 2?



The collector saturation current is:

$$I_{C(SAT)} = \frac{V_{CC}}{R_C + R_E} = \frac{15V}{2.2K + 330\Omega} = 5.93mA$$ (This defines one end of the load line)

The cutoff voltage $V_{CE(OFF)}$ is V_{CC} (15V) (This defines the other end of the load line)

When β = 100:

$$R_{IN(BASE)} = (b+1)R_E = (101)(330\Omega) = 33.33K$$ (This is the *load* on the voltage divider)

The base and emitter voltages are:

$$V_B = V_{CC}\left(\frac{R2 \parallel R_{IN(BASE)}}{R1 + R2 \parallel R_{IN(BASE)}}\right) = 15V\left(\frac{5.6K \parallel 33.33K}{43K + 5.6K \parallel 33.33K}\right) = 1.5V$$

$$V_E = V_B - V_{BE} = 1.5V - 0.7V = 0.8V$$

$$I_E = \frac{V_E}{R_E} = \frac{0.8V}{330\Omega} = 2.42mA$$

$$V_C = V_{CC} - I_C R_C = 15V - (2.42mA)(2.2K) = 9.66V$$

$$g = \frac{V_{CE}}{V_{CC}} = \frac{9.66V - 0.8V}{15V} = \underline{\underline{0.591}}$$

(continued, next page)

When β = 200:

$$R_{IN(BASE)} = (b+1)R_E = (201)(330\Omega) = 66.33K$$ (This is the *load* on the voltage divider)

The base and emitter voltages are:

$$V_B = V_{CC}\left(\frac{R2 \parallel R_{IN(BASE)}}{R1 + R2 \parallel R_{IN(BASE)}}\right) = 15V\left(\frac{5.6K \parallel 66.33K}{43K + 5.6K \parallel 66.33K}\right) = 1.6V$$

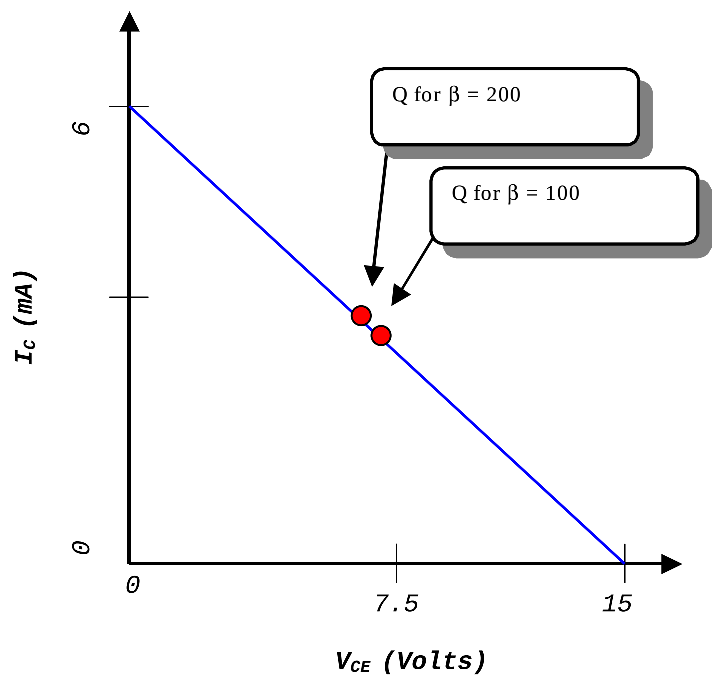
$$V_E = V_B - V_{BE} = 1.6V - 0.7V = 0.9V$$

$$I_E = \frac{V_E}{R_E} = \frac{0.9V}{330\Omega} = 2.73mA$$

$$V_C = V_{CC} - I_C R_C = 15V - (2.73mA)(2.2K) = 9V$$

$$g = \frac{V_{CE}}{V_{CC}} = \frac{9V - 0.8V}{15V} = \underline{\underline{0.547}}$$

The load line with Q-points looks like this:



<u>Comment</u>: The circuit is *much* more stable. Even though β_{DC} doubled in value, the collector current increased by only 0.31 mA (a 12.8% increase when compared to the original current of 2.42 mA).

7. Design a voltage-divider bias circuit to meet the following specifications:

Rc = 10 K $\gamma = 0.5$ Vcc = 15 V
β_{DC} = 150 to 250

Show all calculations and neatly draw the resulting circuit configuration.

Design steps:

1) $V_{CE} = gV_{CC} = (0.5)(15V) = 7.5V$

2) $V_E = 1V$

3) $V_C = V_E + V_{CE} = 1V + 7.5V = 8.5V$

4) $I_E \approx I_C = \dfrac{V_{CC} - V_C}{R_C} = \dfrac{15V - 8.5V}{10K} = 0.65mA$

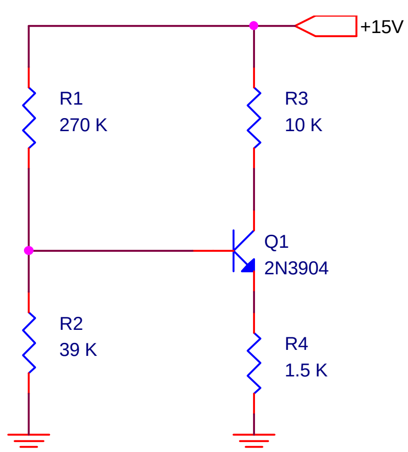
5) $R_E = \dfrac{V_E}{I_E} = \dfrac{1V}{0.65mA} = 1538\Omega$ (1.5 K Ω standard)

6) $I_B = \dfrac{I_E}{(b_{DC(MIN)} + 1)} = \dfrac{0.65mA}{(150+1)} = 4.3mA$

7)
$$IR_2 = 10I_B$$
$$\therefore R_2 = \frac{V_B}{10I_B} = \frac{1V + 0.7V}{10(4.3mA)} = \underline{\underline{39.534K}}$$
(R2 = 39 K standard)

8)
$$IR_1 = 11I_B$$
$$\therefore R_1 = \frac{(V_{CC} - V_B)}{11I_B} = \frac{(15V - 1.7V)}{11(4.3mA)} = \underline{\underline{281.183K}}$$
(R1 = 270 K standard)

The circuit looks like this:



Design verification by CESIM software (not required of student)

Vcc = 15.00 Volts , BetaDC = 150.00
RB1 = 270000.0 Ohms, RB2 = 39000.0 Ohms
RC = 10000.0
Re1 = 1500.0, Re2 = 0.0

DC Parameters:

VB = 1.65 Volts, VE = 0.95 Volts, VC = 8.74 Volts
IE = 0.63 mA, IC = 0.63 mA
Total DC Input Power = 10.12 mW
Device power dissipation PD = 4.88 mW

8. Design a voltage-divider bias circuit to meet the following specifications:

Rc = 5.6 K $\qquad$ γ = 0.3 $\qquad$ Vcc = 40 V
β_{DC} = 100 to 400

Show all calculations and neatly draw the resulting circuit configuration.

Design steps:

1) $V_{CE} = gV_{CC} = (0.3)(40V) = 12V$

2) $V_E = 1V$

3) $V_C = V_E + V_{CE} = 1V + 12V = 13V$

4) $I_E \approx I_C = \dfrac{V_{CC} - V_C}{R_C} = \dfrac{40V - 13V}{5.6K} = 4.82mA$

5) $R_E = \dfrac{V_E}{I_E} = \dfrac{1V}{4.82mA} = 207.4\Omega$ (220 Ω standard)

6) $I_B = \dfrac{I_E}{(b_{DC(MIN)} + 1)} = \dfrac{4.82mA}{(100+1)} = 47.73mA$

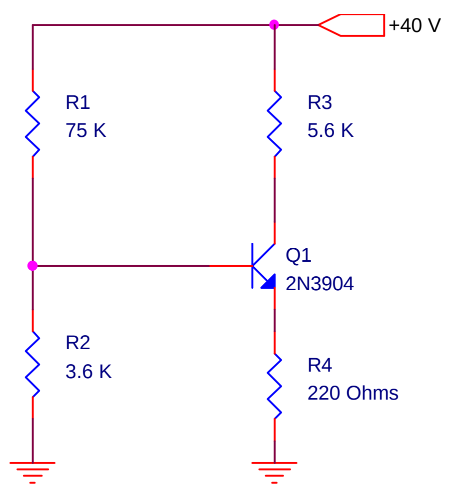
7) $IR_2 = 10I_B$

$\therefore R_2 = \dfrac{V_B}{10I_B} = \dfrac{1V + 0.7V}{10(47.73mA)} = 3.561K$ (R2 = 3.6 K standard)

8) $IR_1 = 11I_B$

$\therefore R_1 = \dfrac{(V_{CC} - V_B)}{11I_B} = \dfrac{(40V - 1.7V)}{11(47.73mA)} = 72.937K$ (R1 = 75 K standard)

The circuit looks like this:



Design verification by CESIM software (not required of student)

Vcc = 40.00 Volts , BetaDC = 100.00
RB1 = 75000.0 Ohms, RB2 = 3600.0 Ohms
RC = 5600.0
Re1 = 220.0, Re2 = 0.0

DC Parameters:

VB = 1.59 Volts, VE = 0.89 Volts, VC = 17.65 Volts
IE = 4.03 mA, IC = 3.99 mA
Total DC Input Power = 179.99 mW
Device power dissipation PD = 66.90 mW